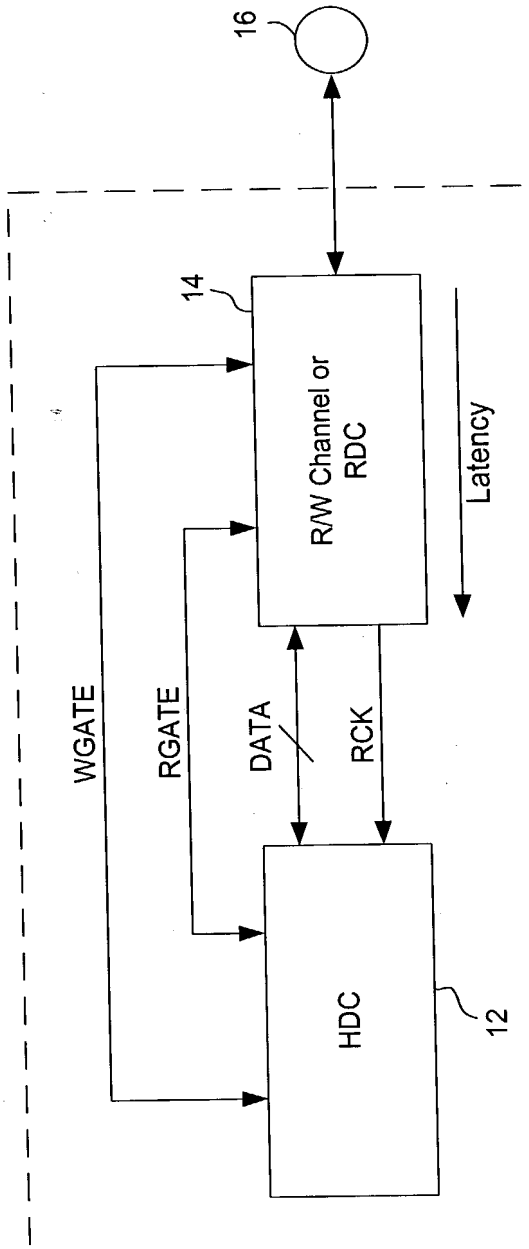

Fig. 1

09759151.091902

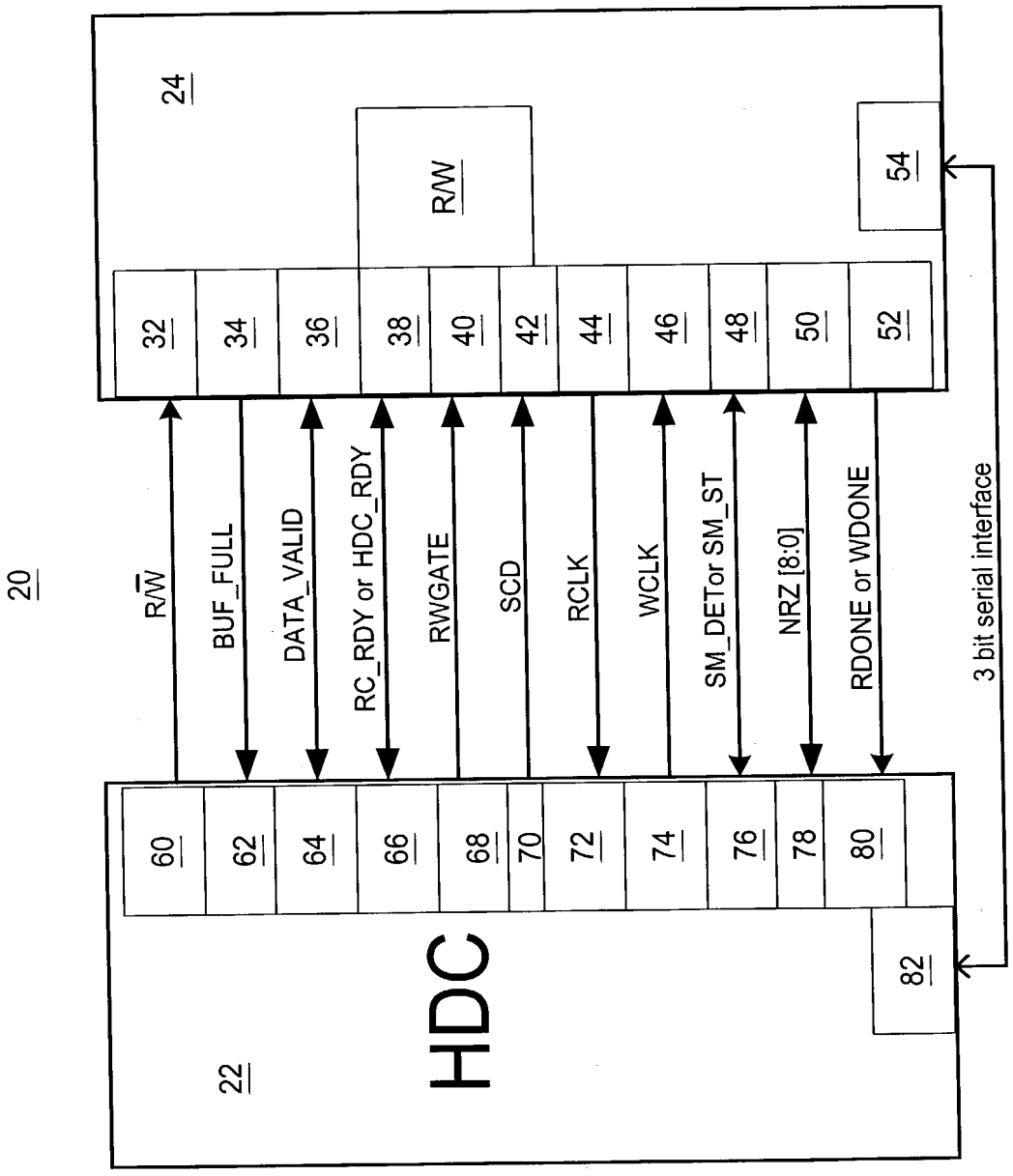

Fig. 2

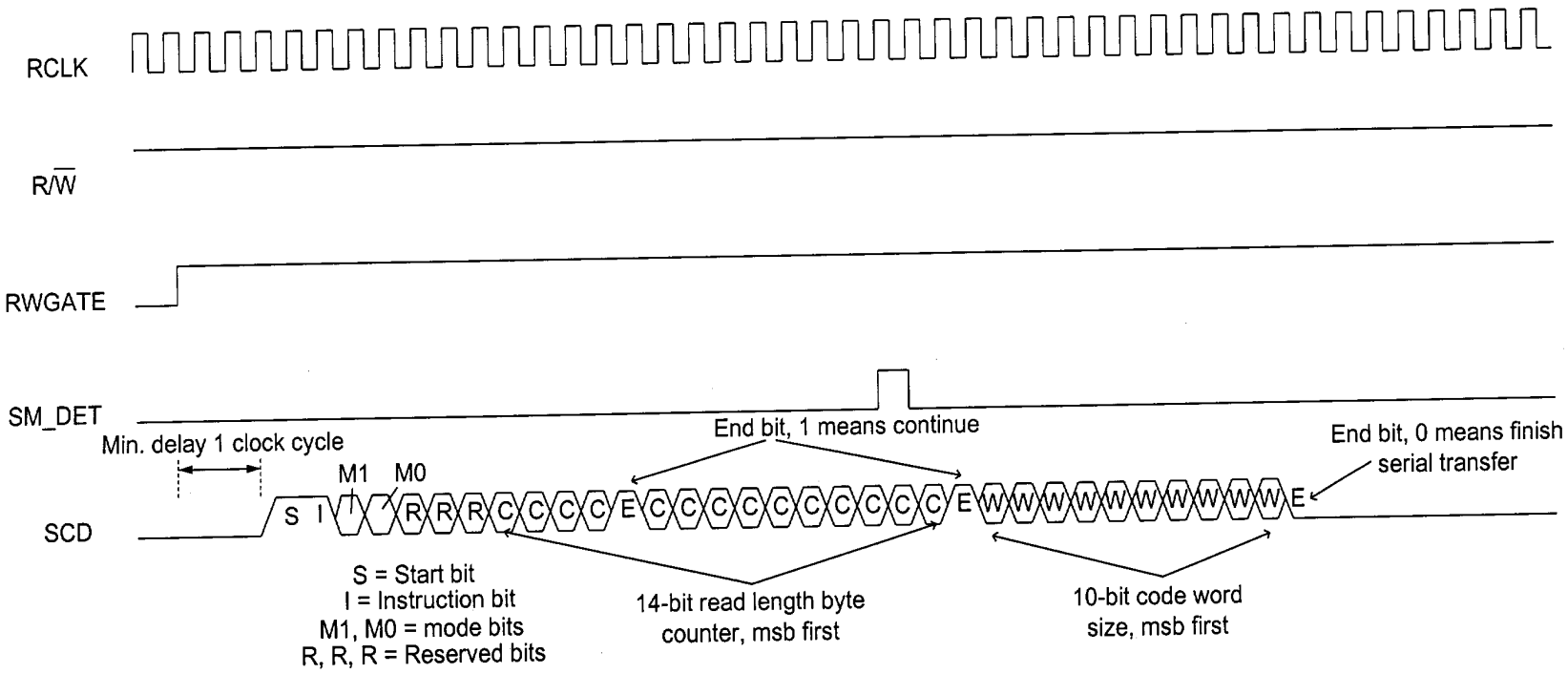

Fig. 3

MP0071
09/759151
Lam
3/37

09759151.091902

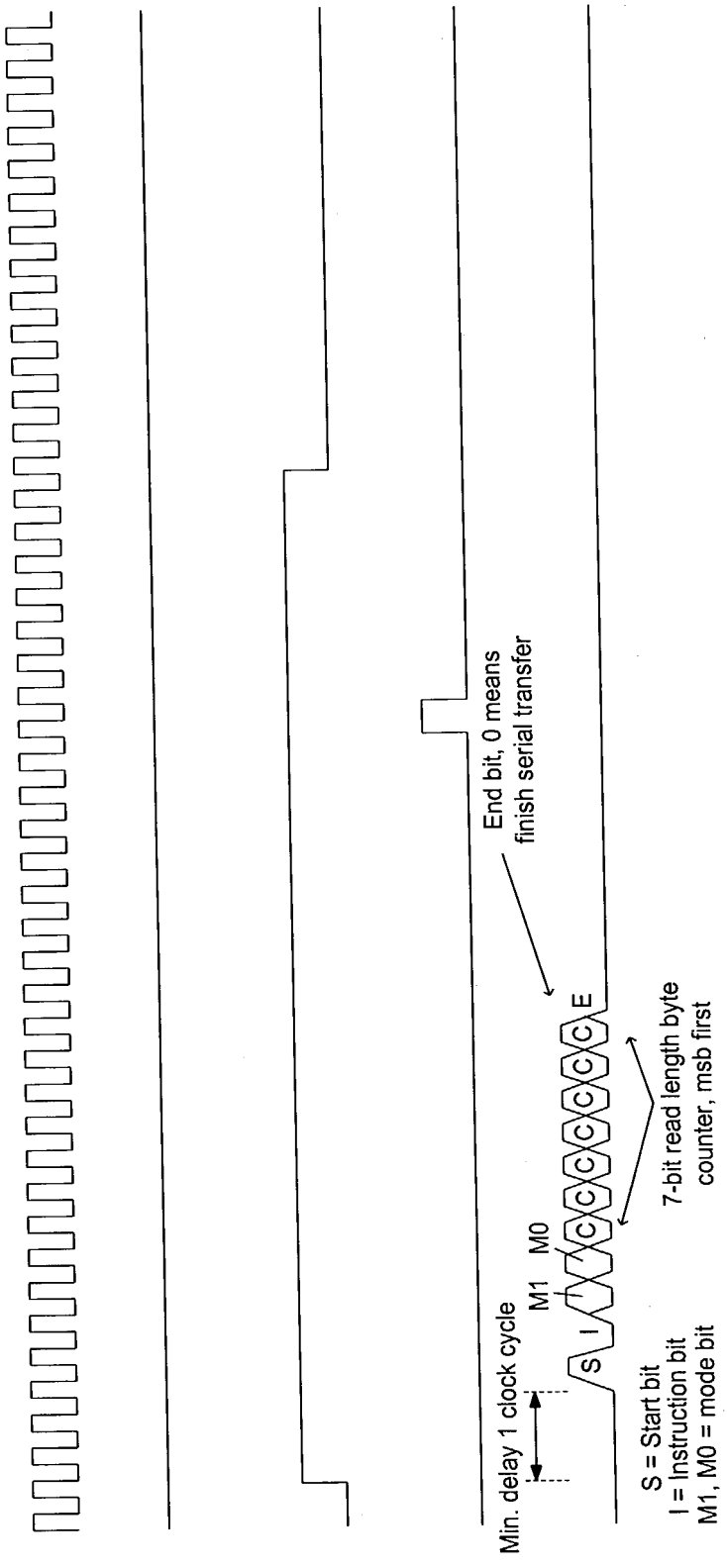

Fig. 4

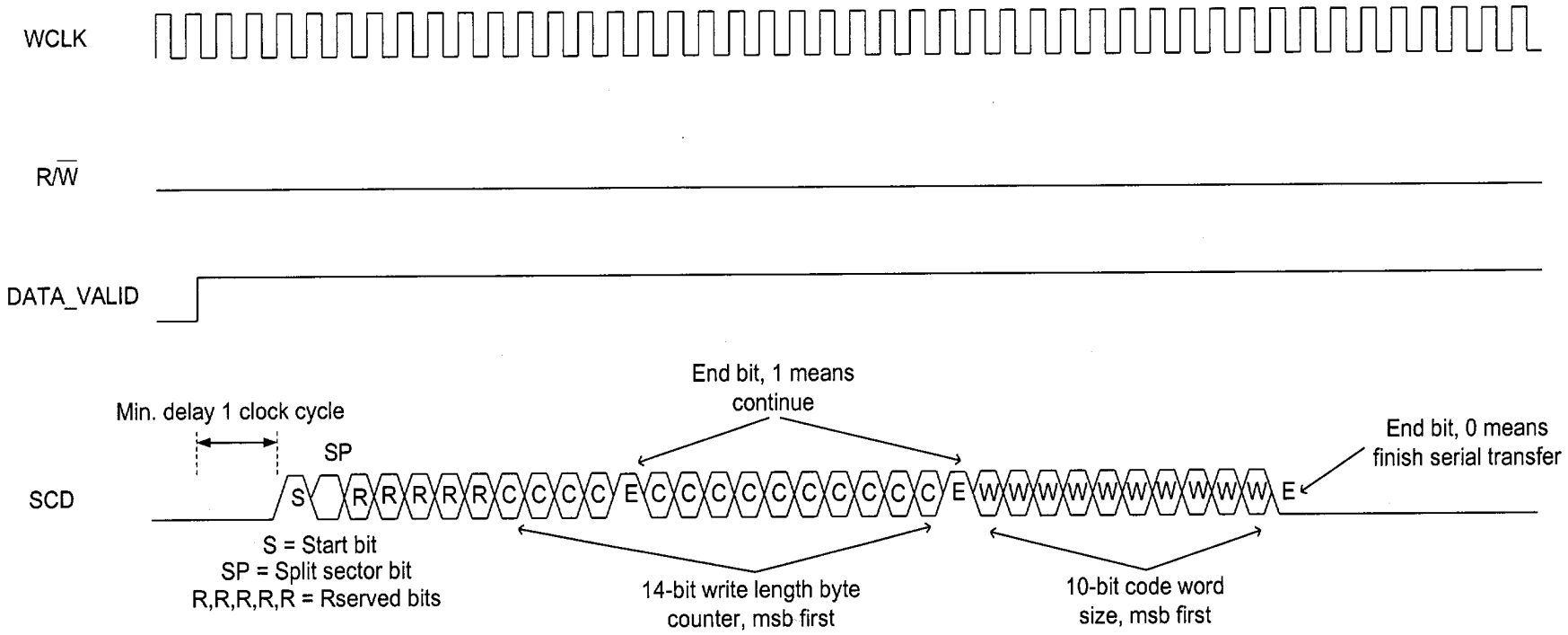

Fig. 5

MP0071
09/759151
Lam
5/37

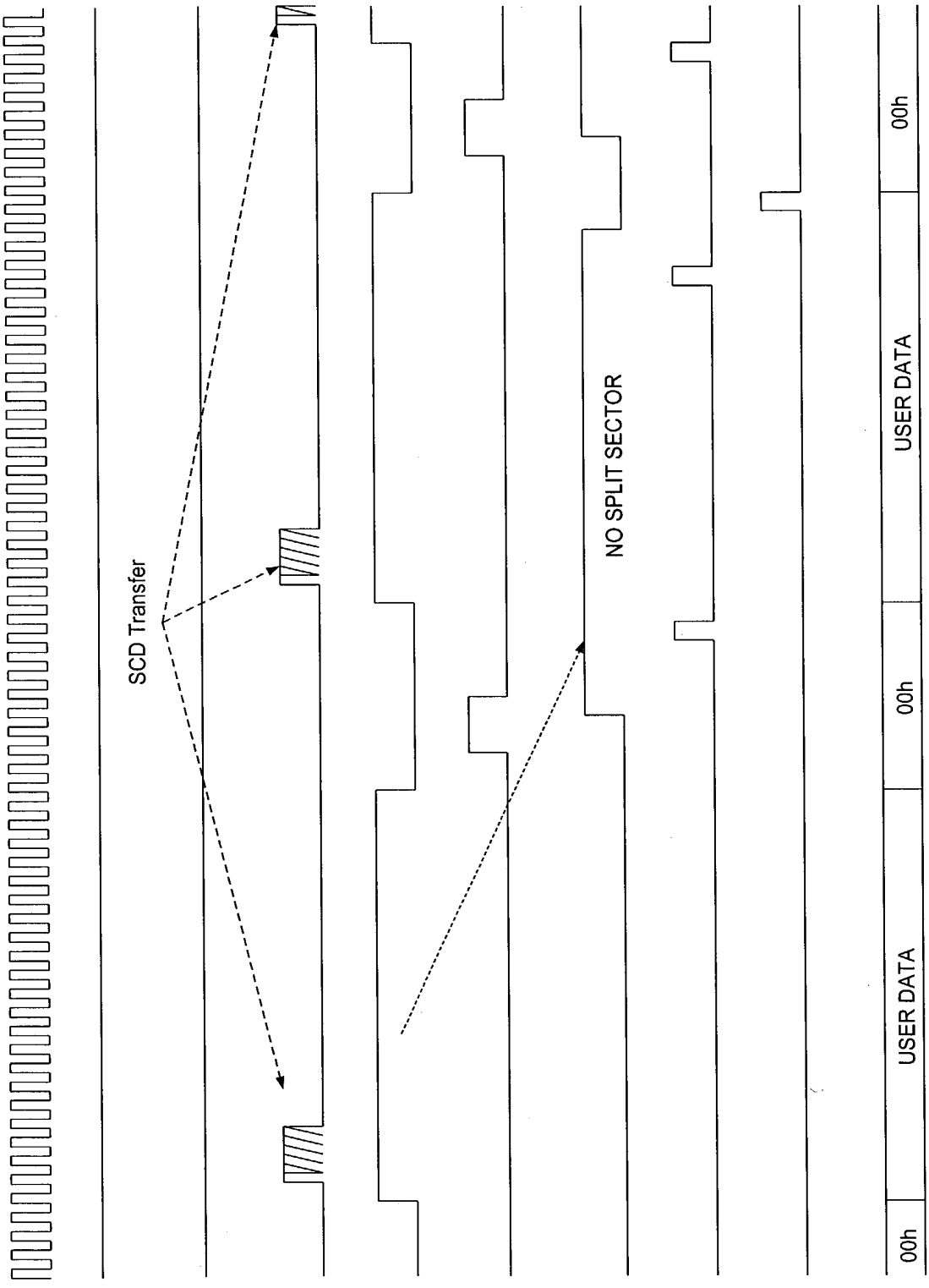
WCLK
R/W
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
SM_ST
WDONE
NRZ[7:0]
SCD Transfer
NO SPLIT SECTOR
00h
USER DATA
00h
USER DATA
00h

Fig. 6

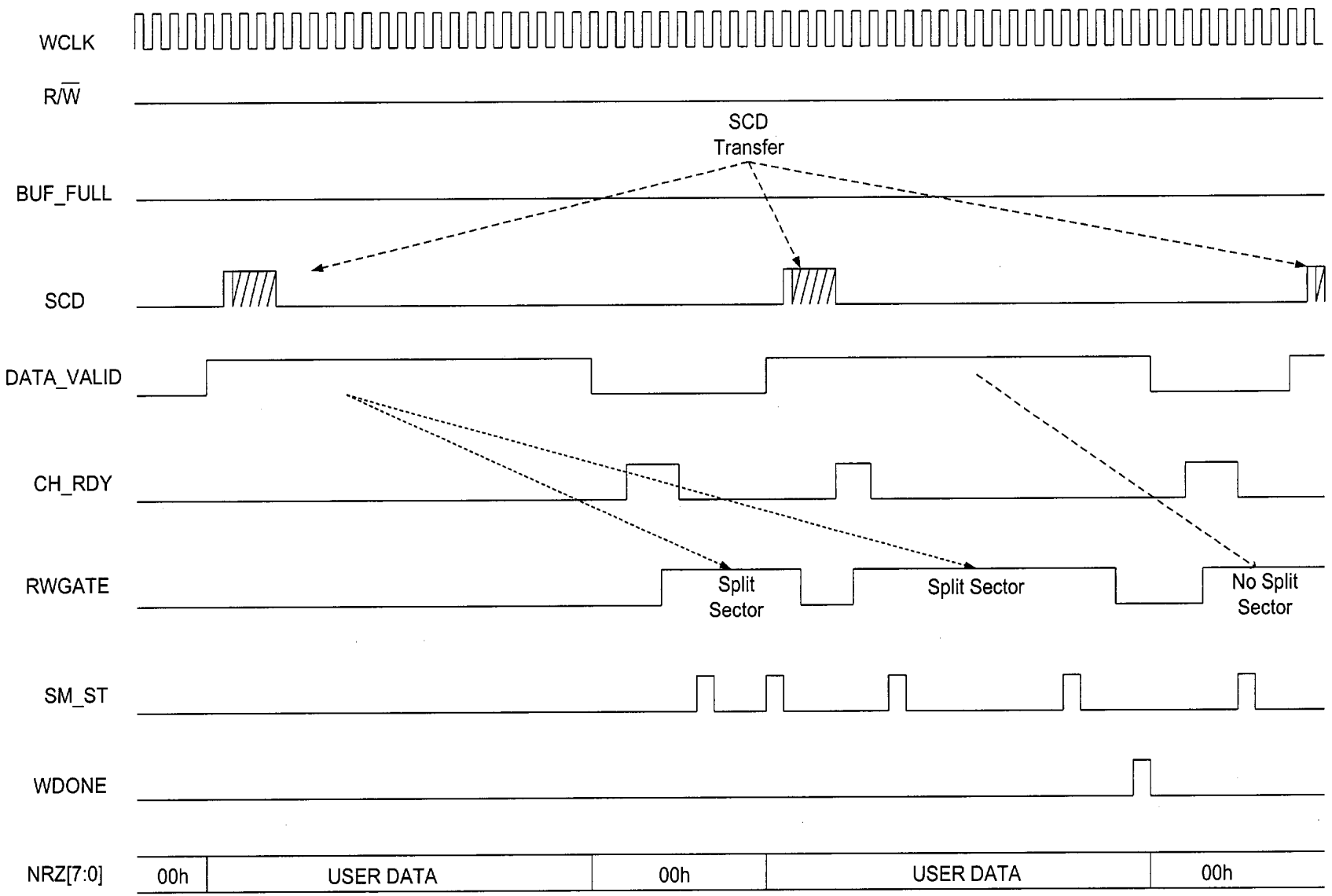
WCLK
R/W
SCD
Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
Split
Sector
Split Sector
No Split
Sector
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 7

09759151.091902

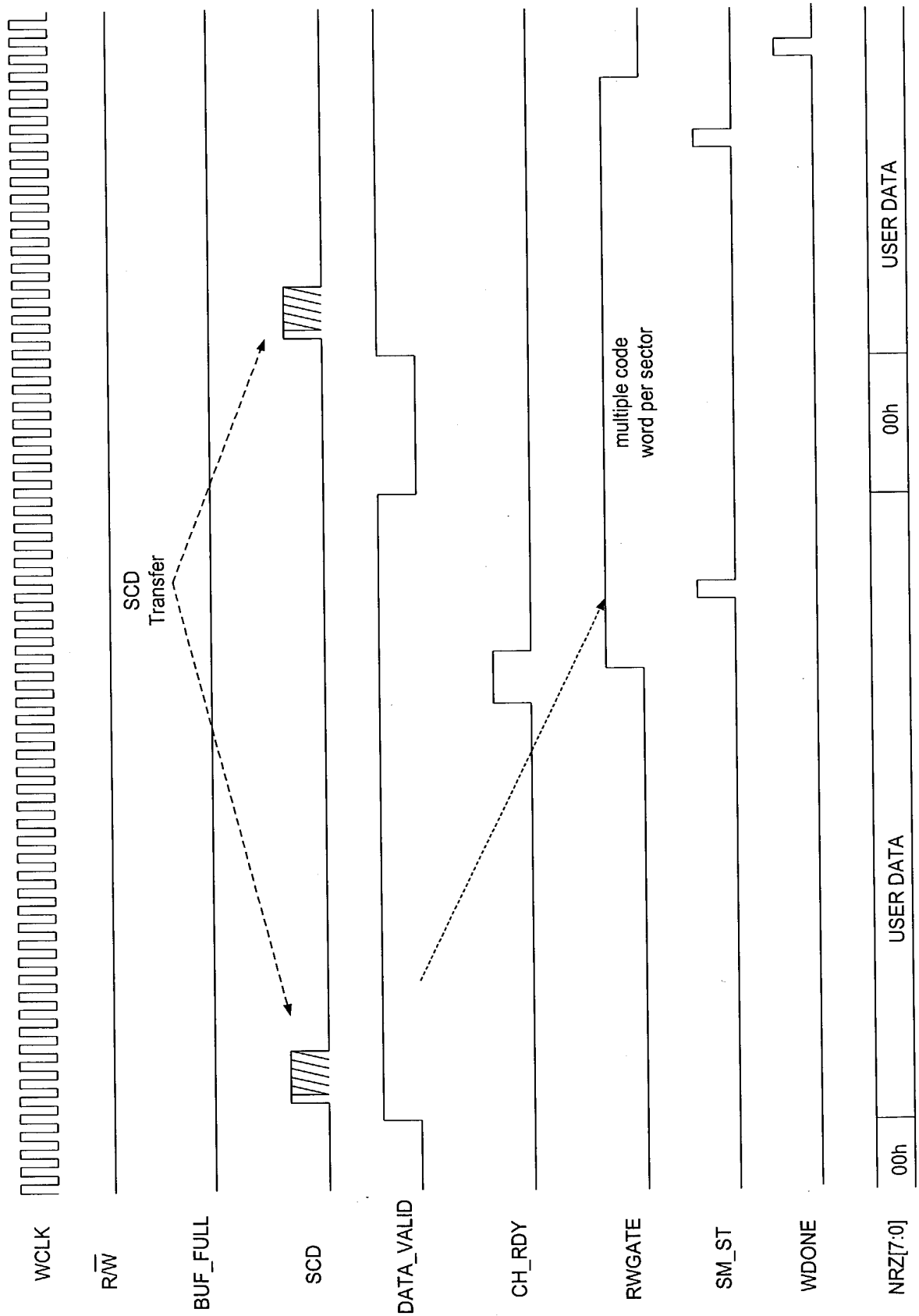

Fig. 8

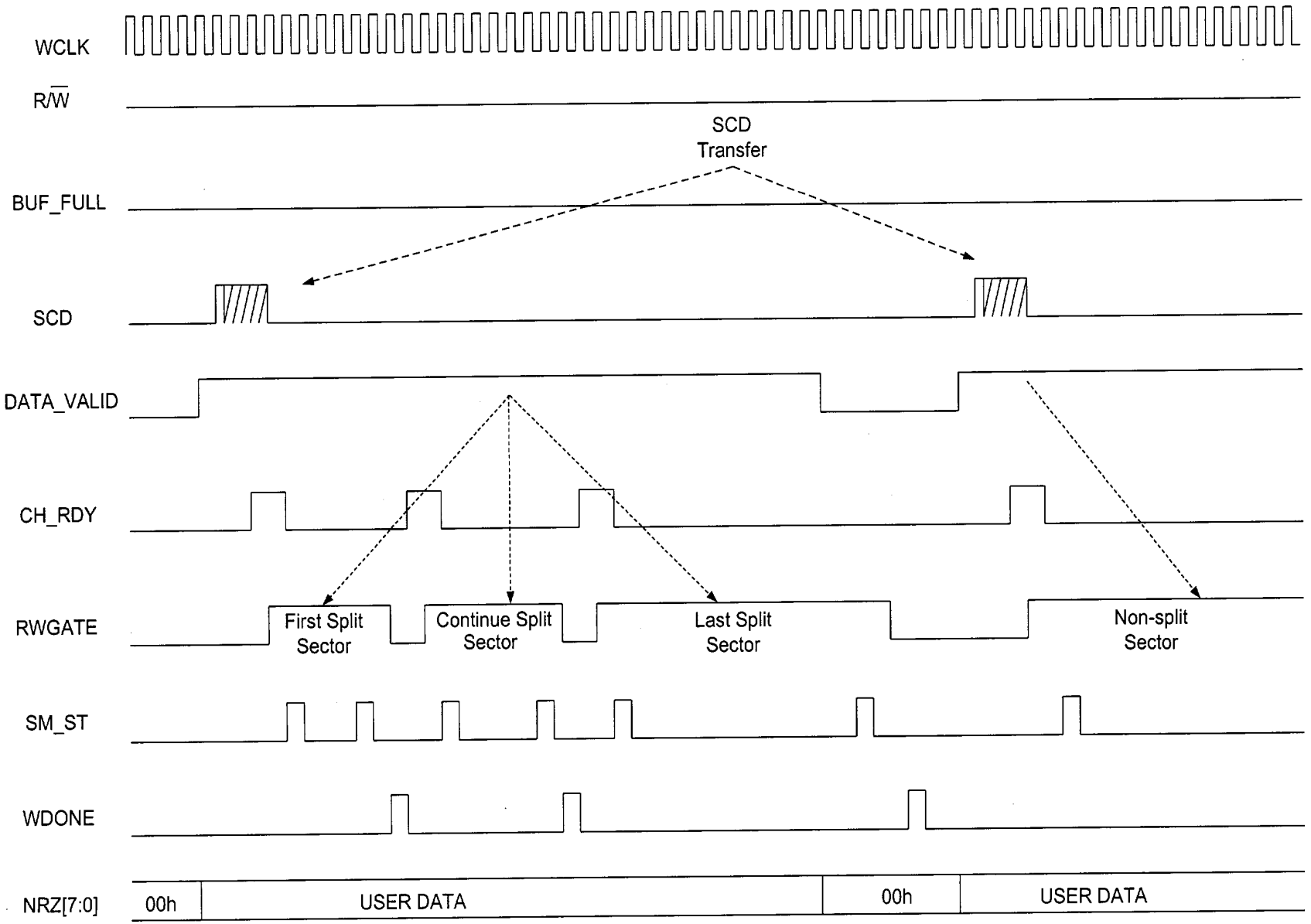
WCLK
R/W
SCD
Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
First Split
Sector
Continue Split
Sector
Last Split
Sector
Non-split
Sector
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 9

09759151.091902

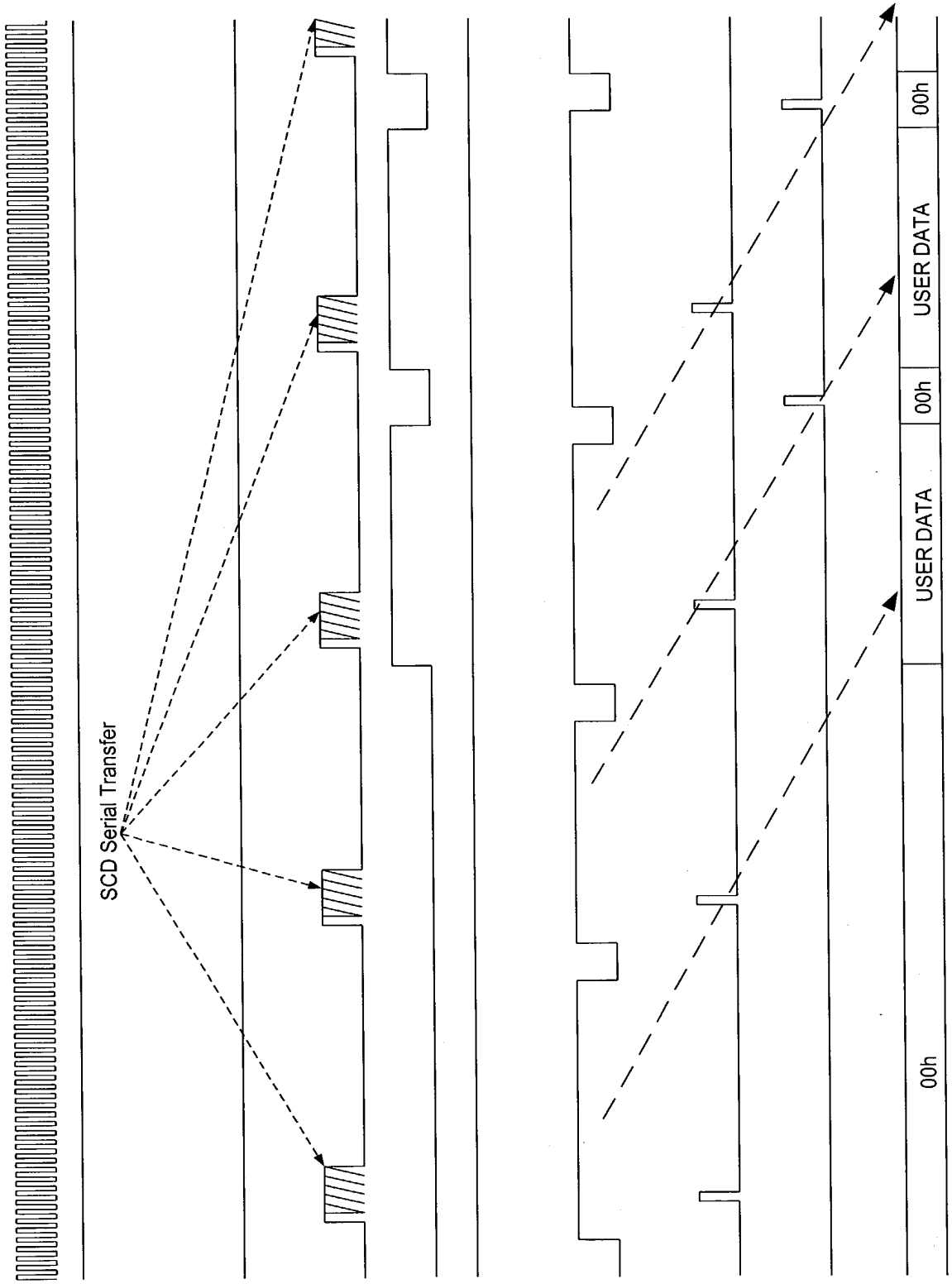

Fig. 10

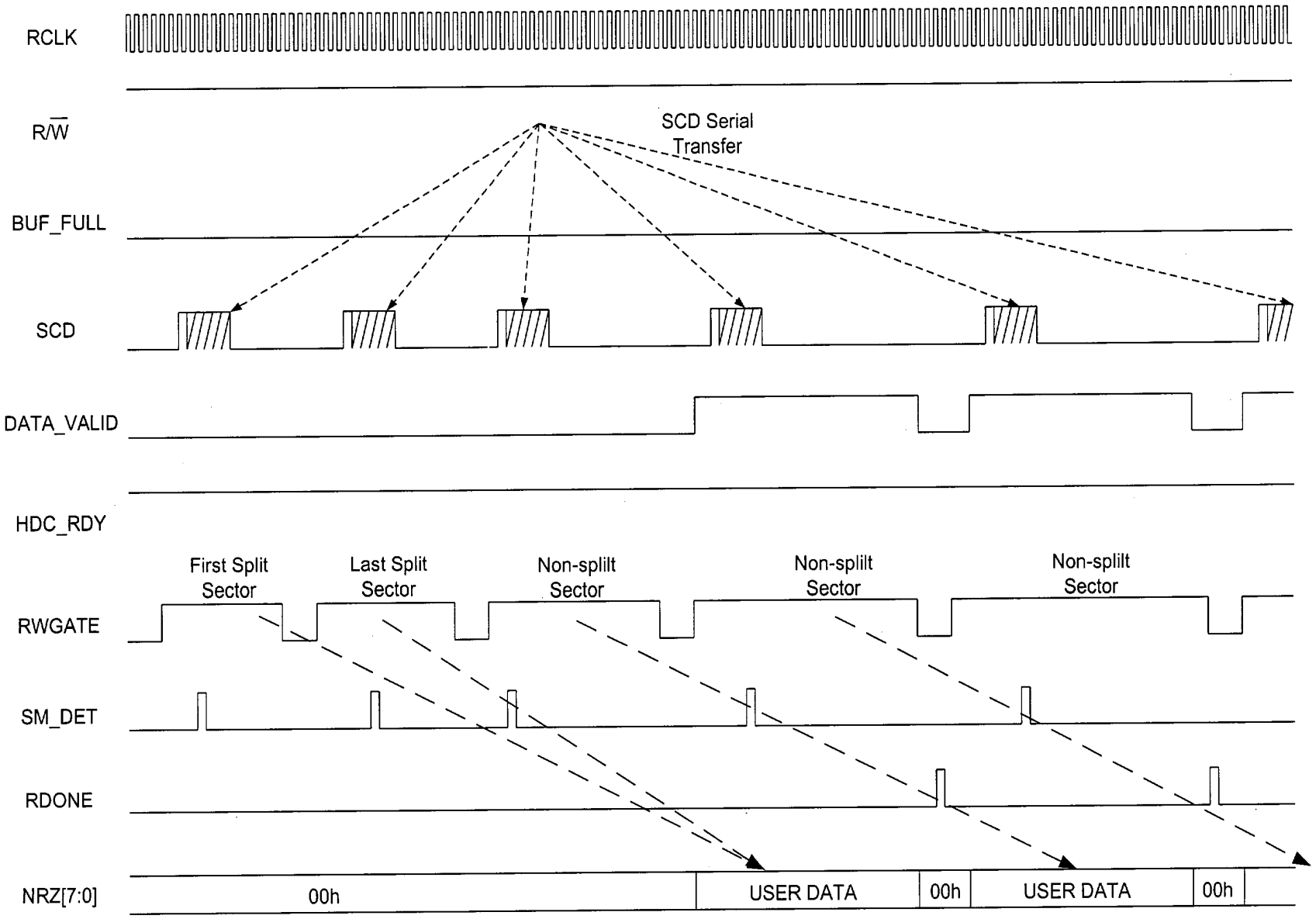
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
First Split Sector
Last Split Sector
Non-splilt Sector
Non-splilt Sector
Non-splilt Sector
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 11

09759151.091902

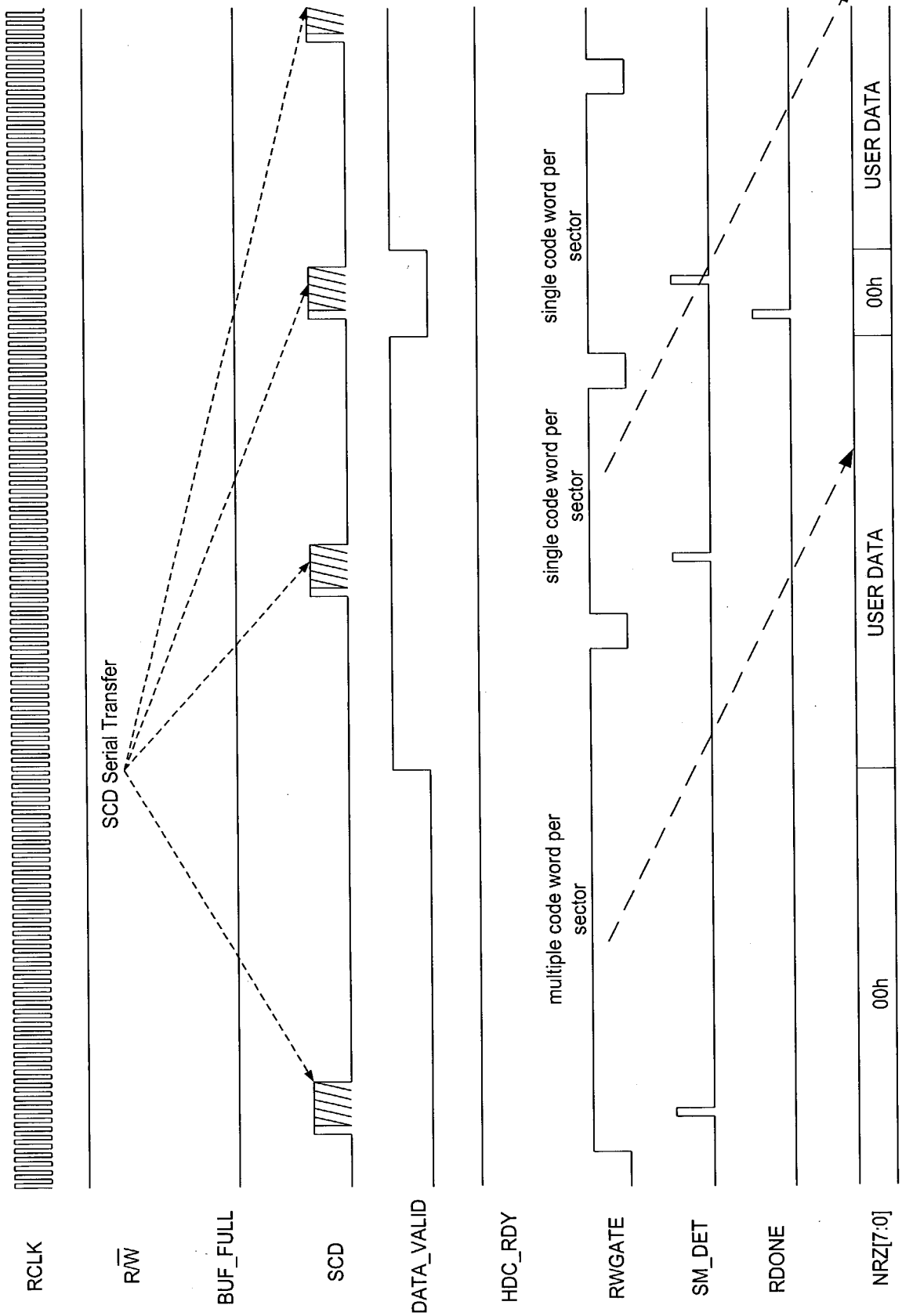

Fig. 12

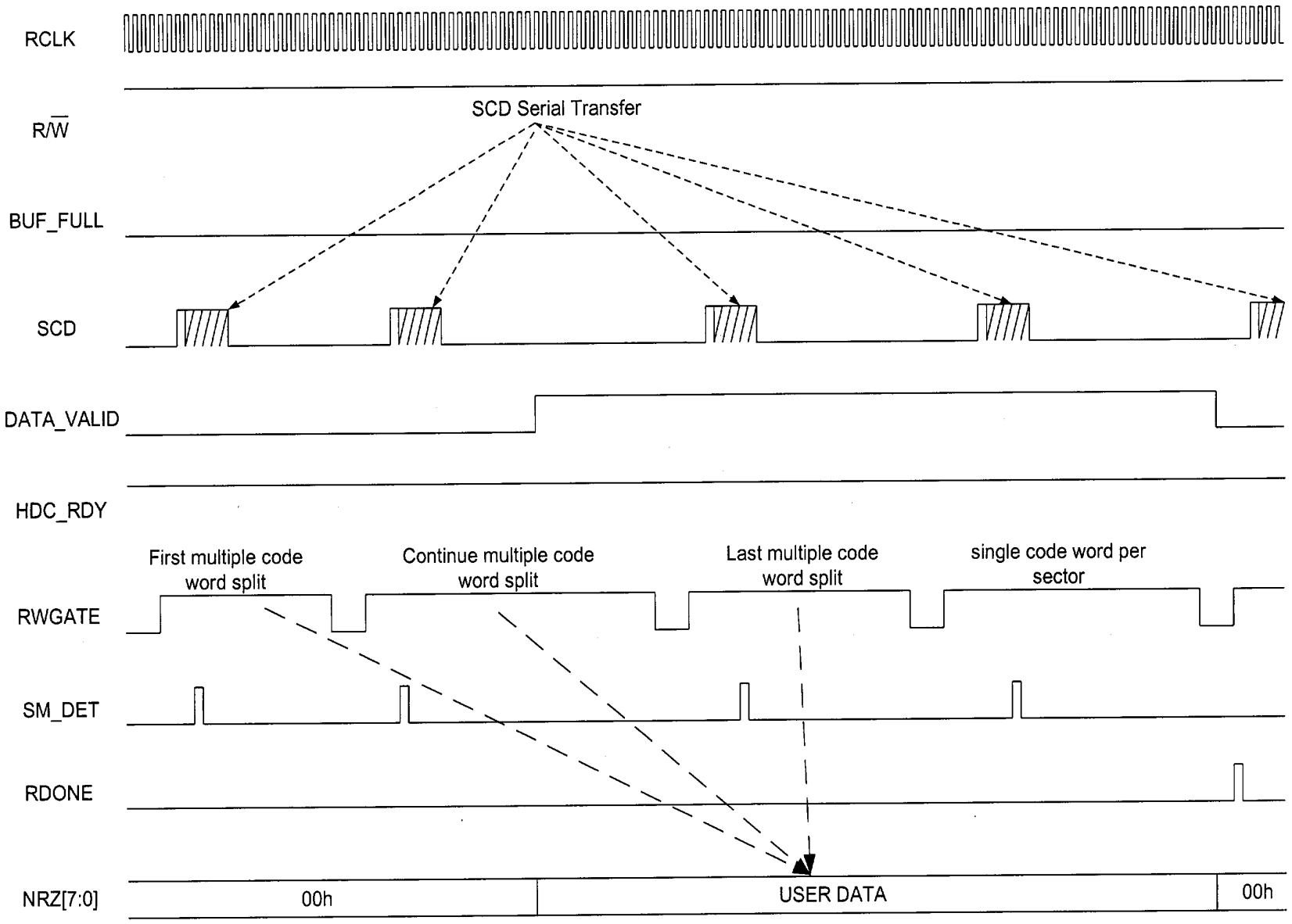
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
First multiple code word split
Continue multiple code word split
Last multiple code word split
single code word per sector
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h

Fig. 13

09759151.091902

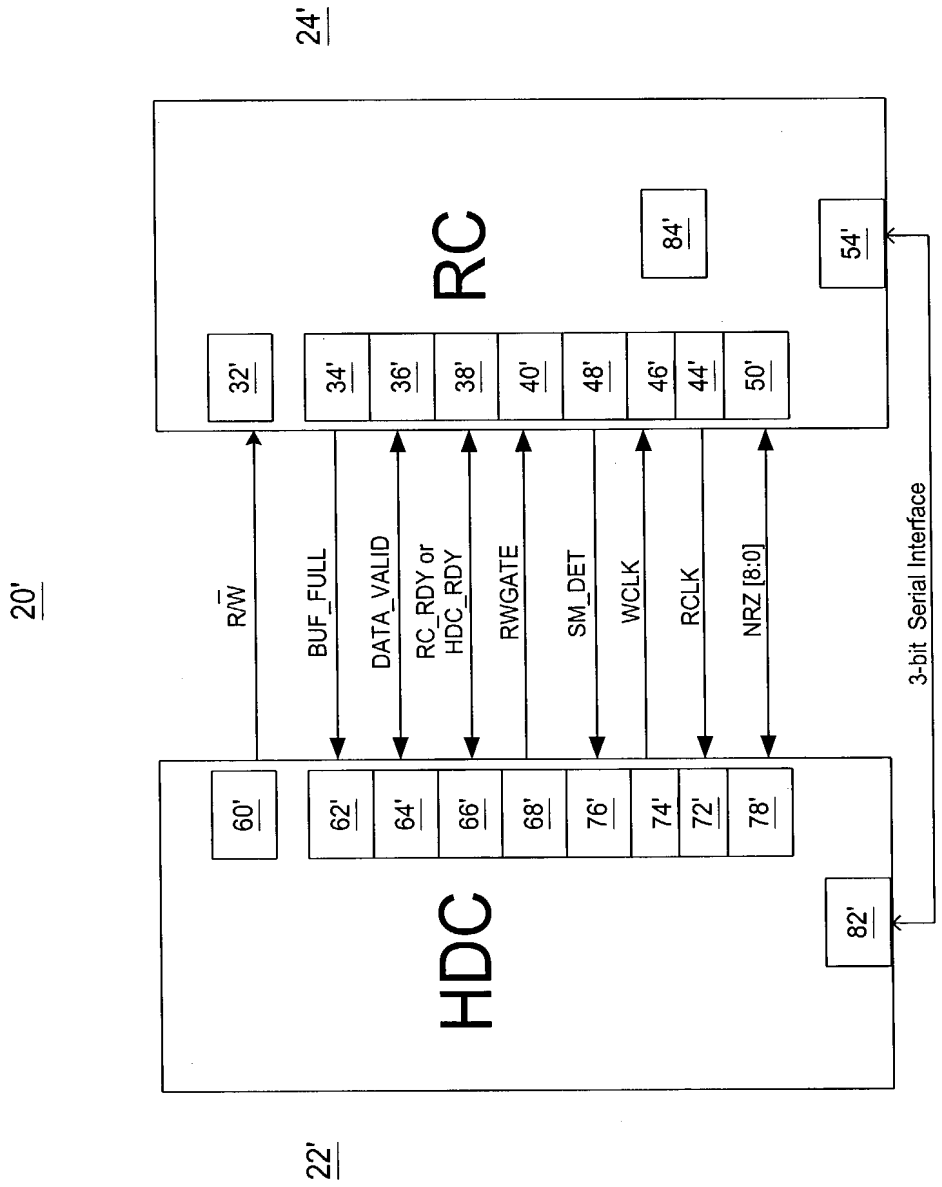

Fig. 14

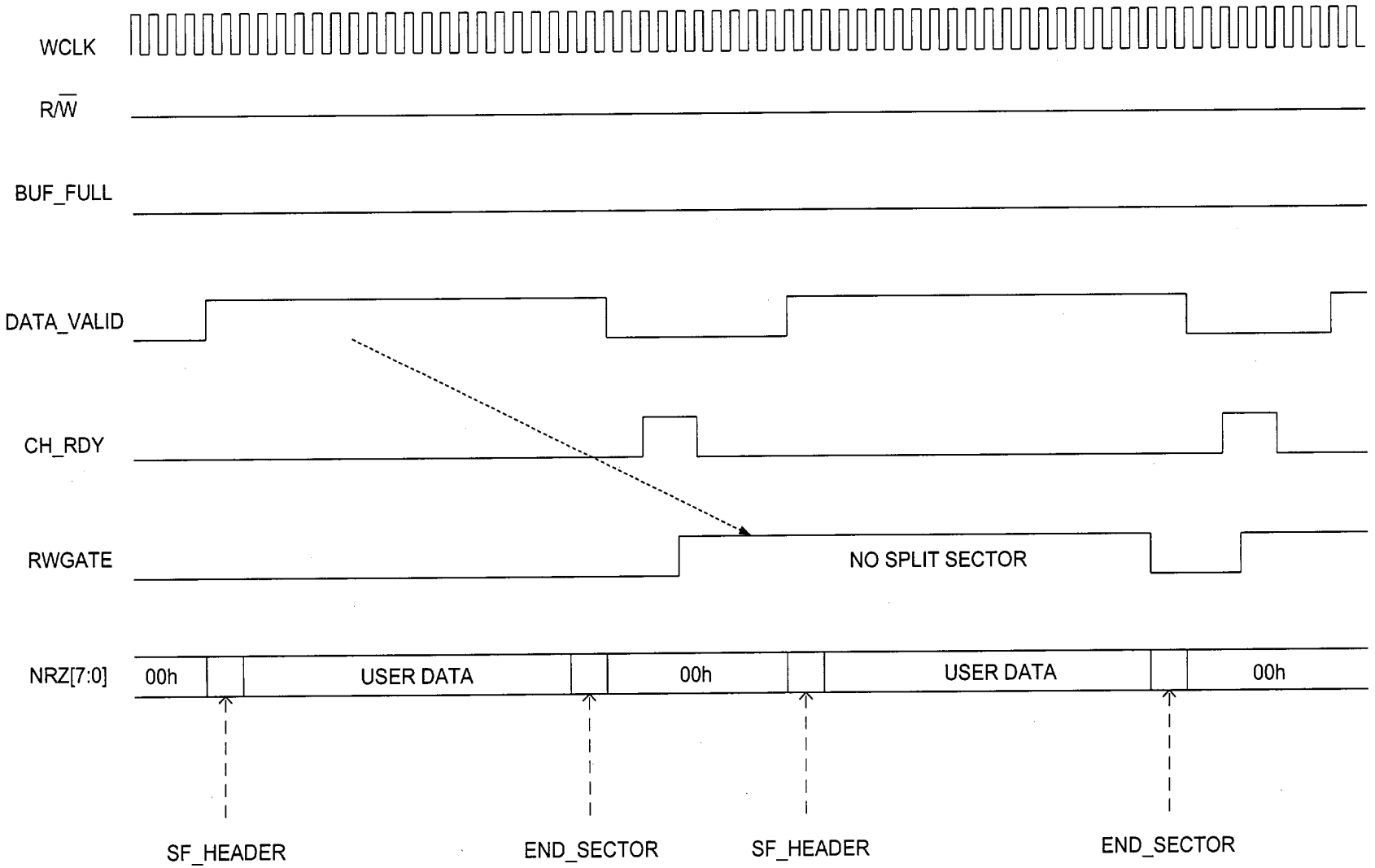
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
NO SPLIT SECTOR
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h
SF_HEADER
END_SECTOR
SF_HEADER
END_SECTOR

Fig. 15

09759151.091902

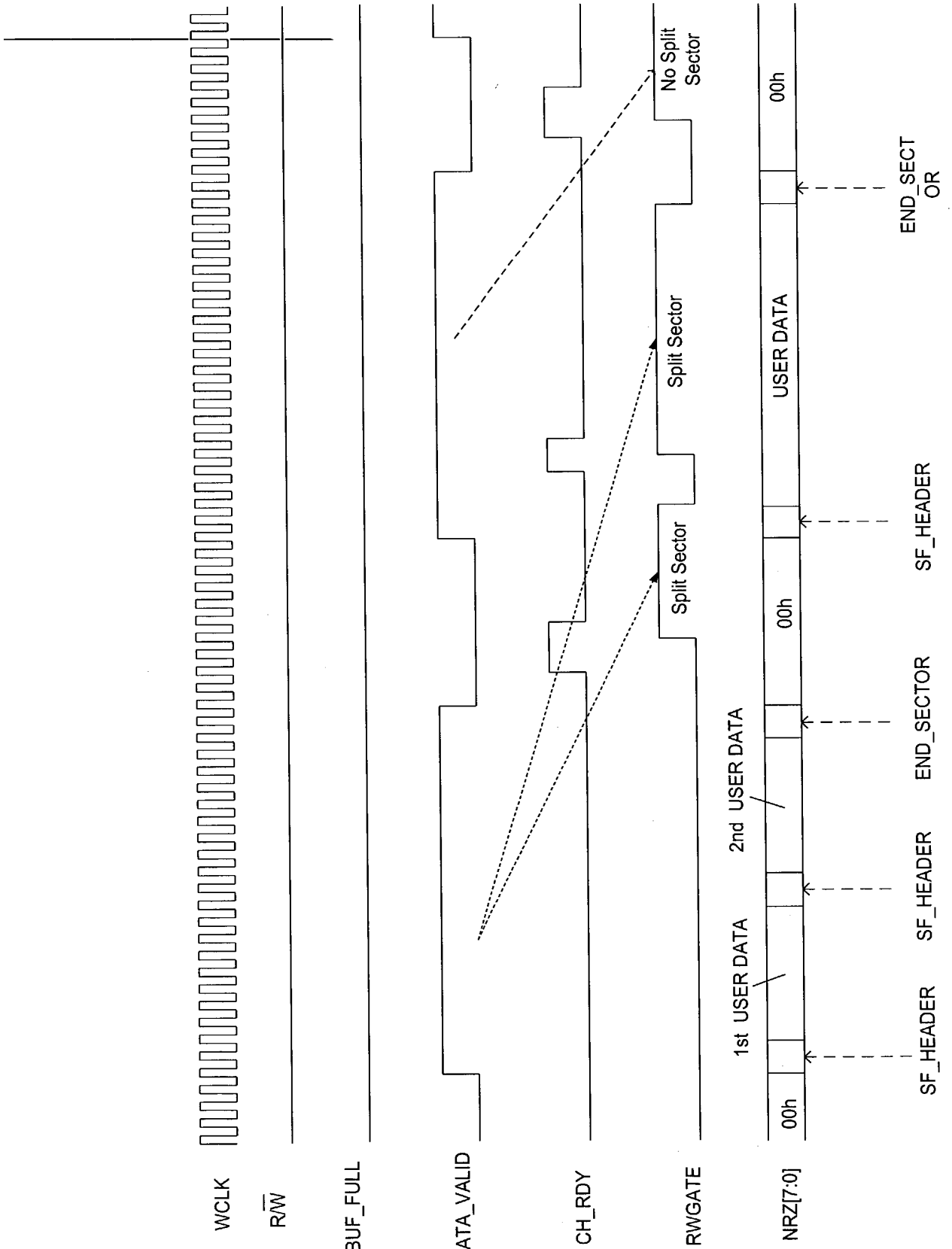

Fig. 16

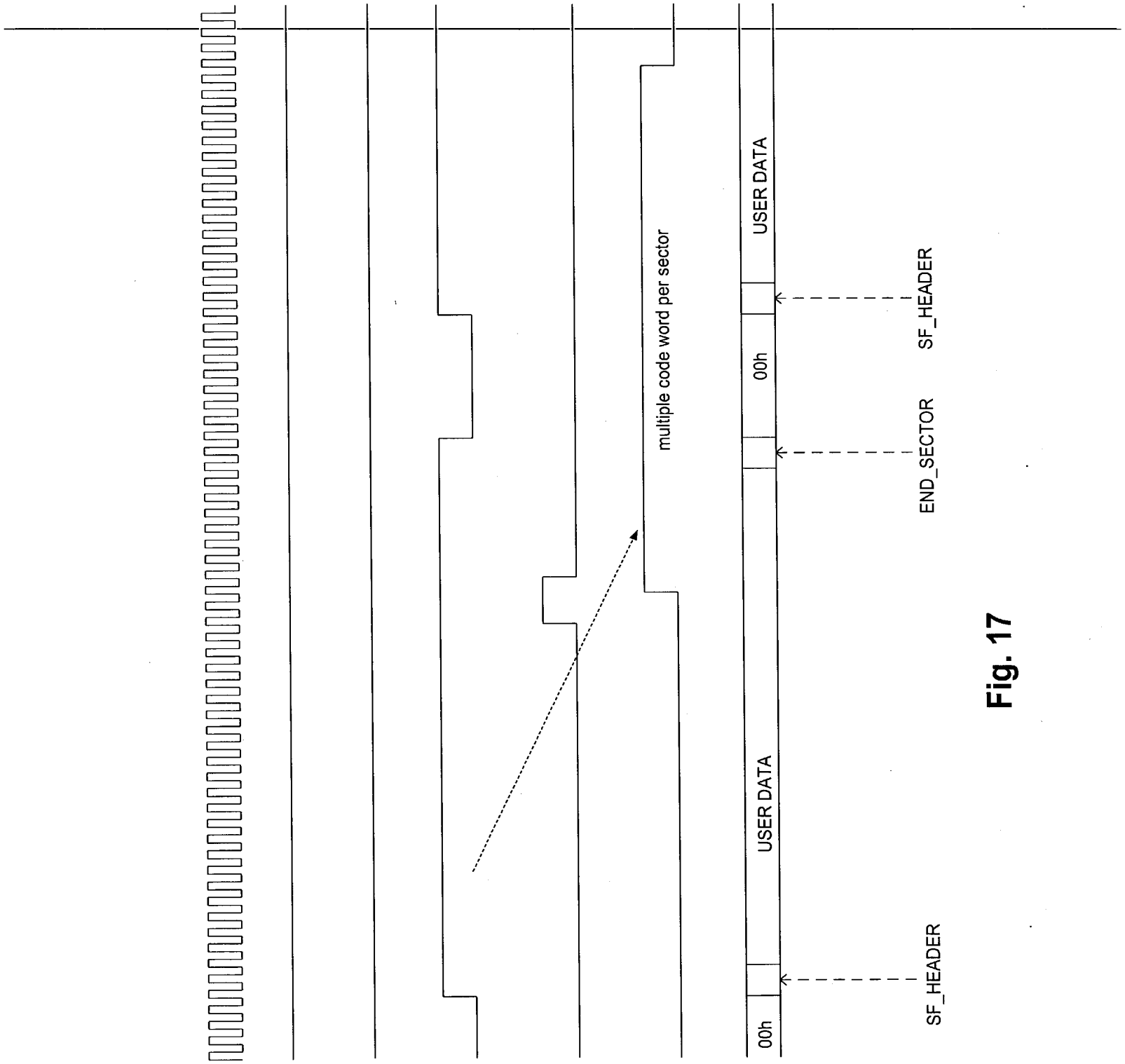
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
NRZ[7:0]
00h
USER DATA
SF_HEADER
multiple code word per sector
USER DATA
00h
END_SECTOR
SF_HEADER

Fig. 17

09759151.091902

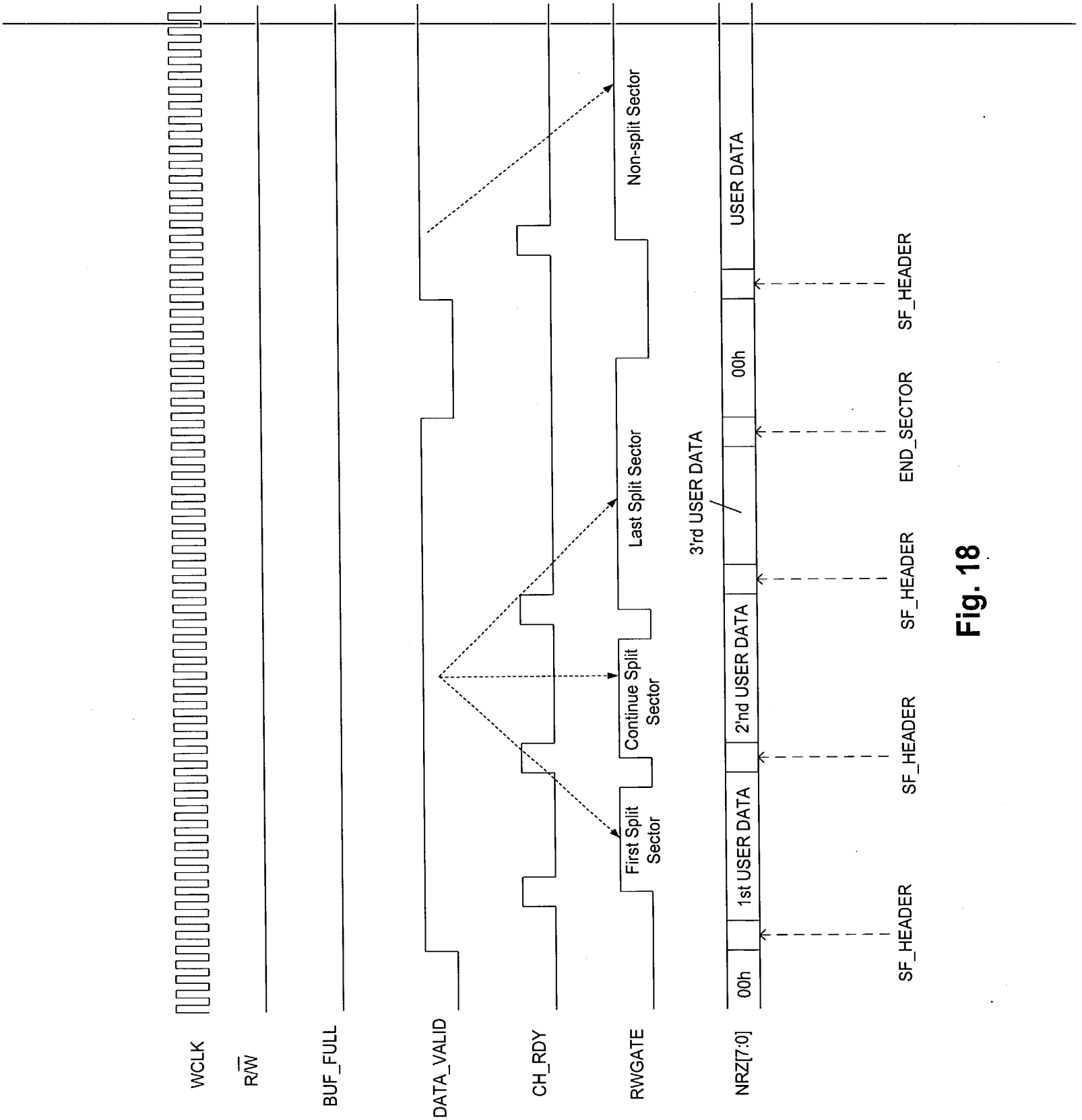

Fig. 18

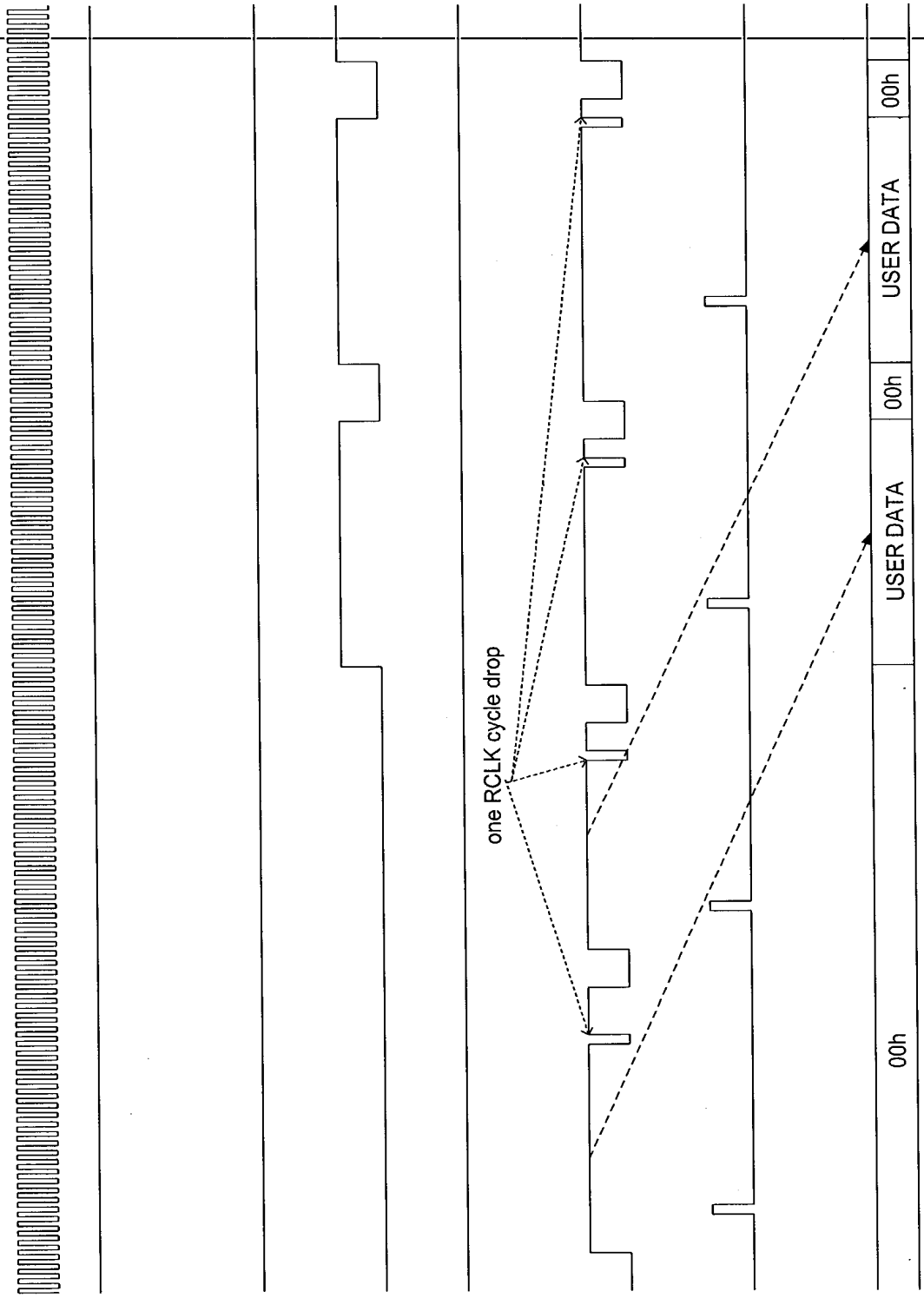
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
RWGATE
SM_DET
NRZ[7:0]
one RCLK cycle drop
00h
USER DATA
00h
USER DATA
00h

Fig. 19

09759151.091902

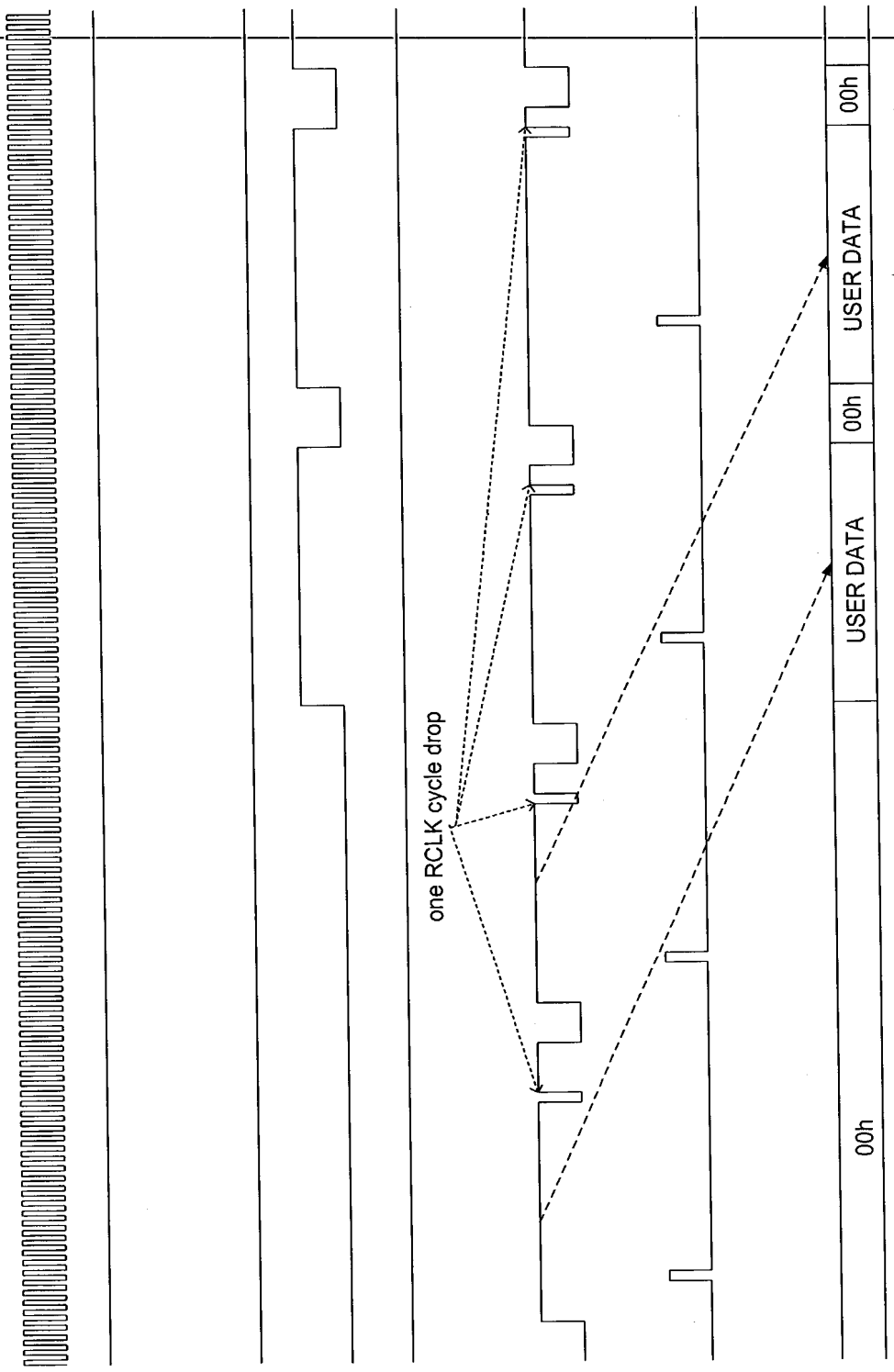

Fig. 20

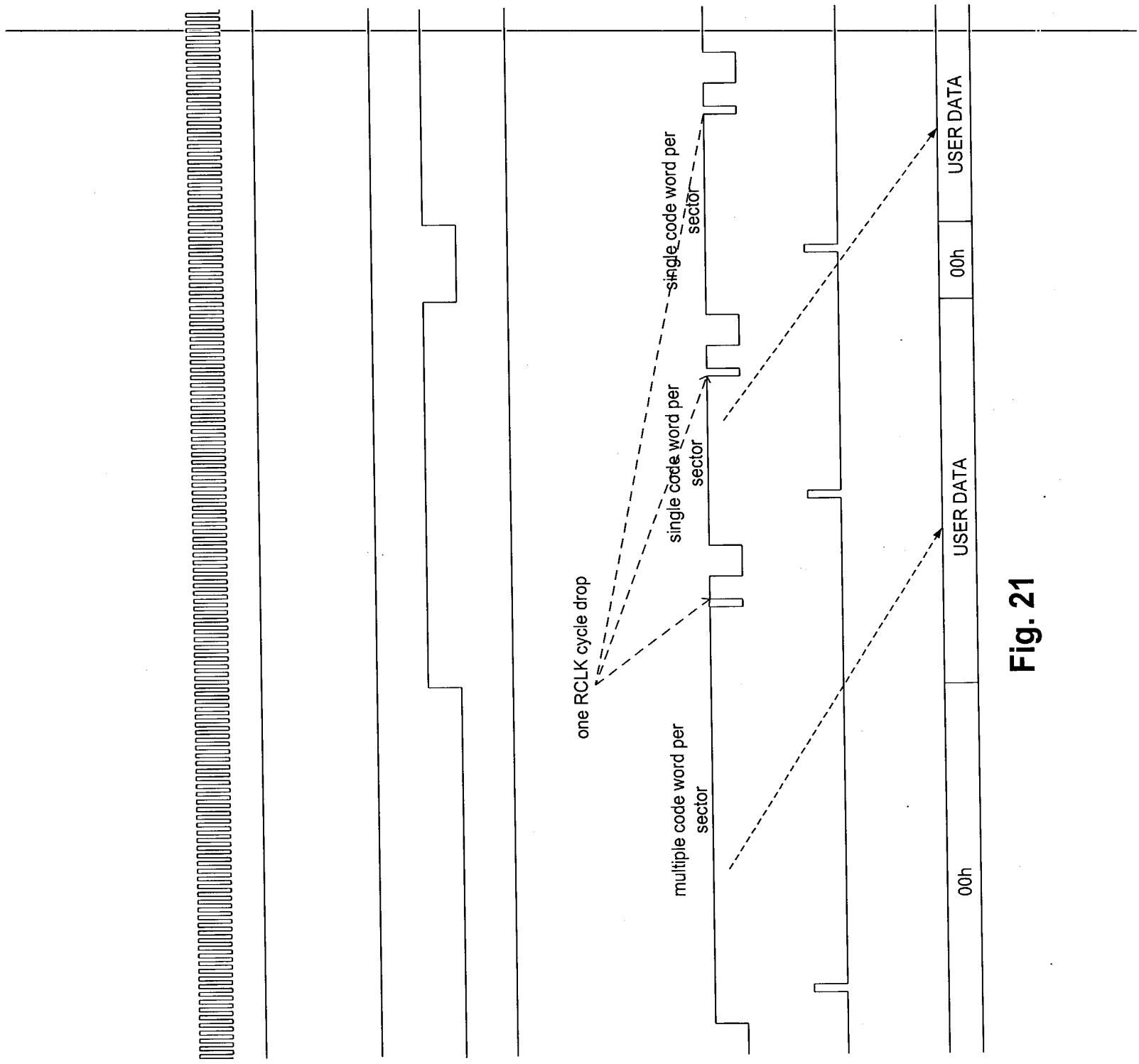
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
RWGATE
SM_DET
NRZ[7:0]
one RCLK cycle drop
single code word per sector
single code word per sector
multiple code word per sector
00h
USER DATA
00h
USER DATA

Fig. 21

09759151.091902

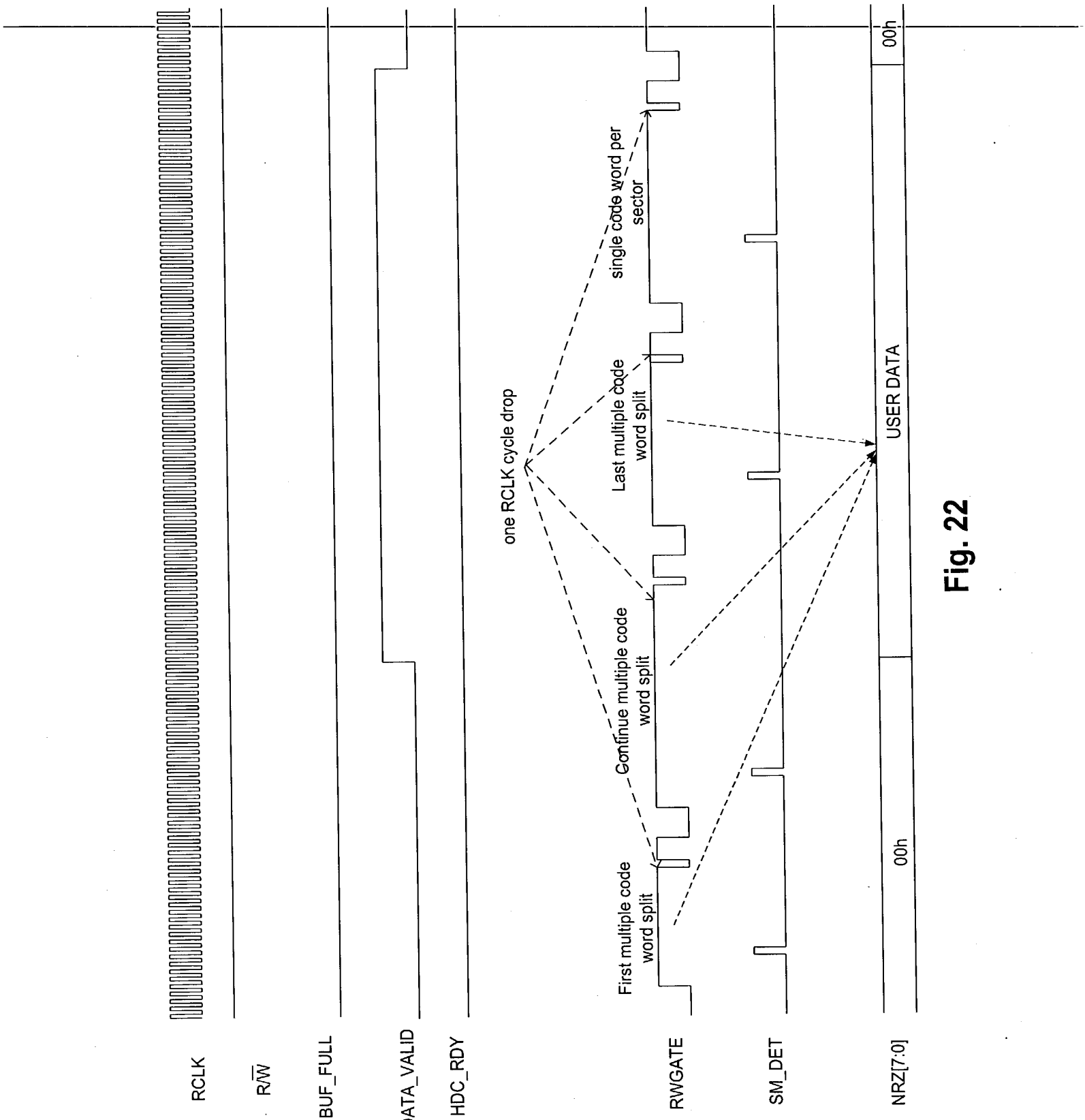

Fig. 22

09759151.091902

Fig. 23

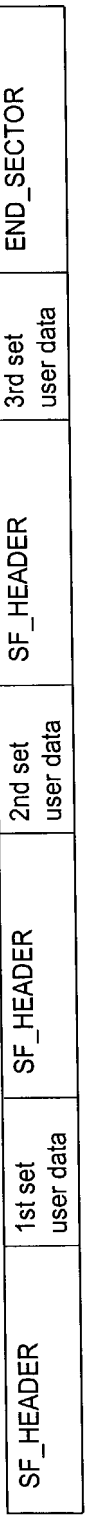

Fig. 24

09759151 .091902

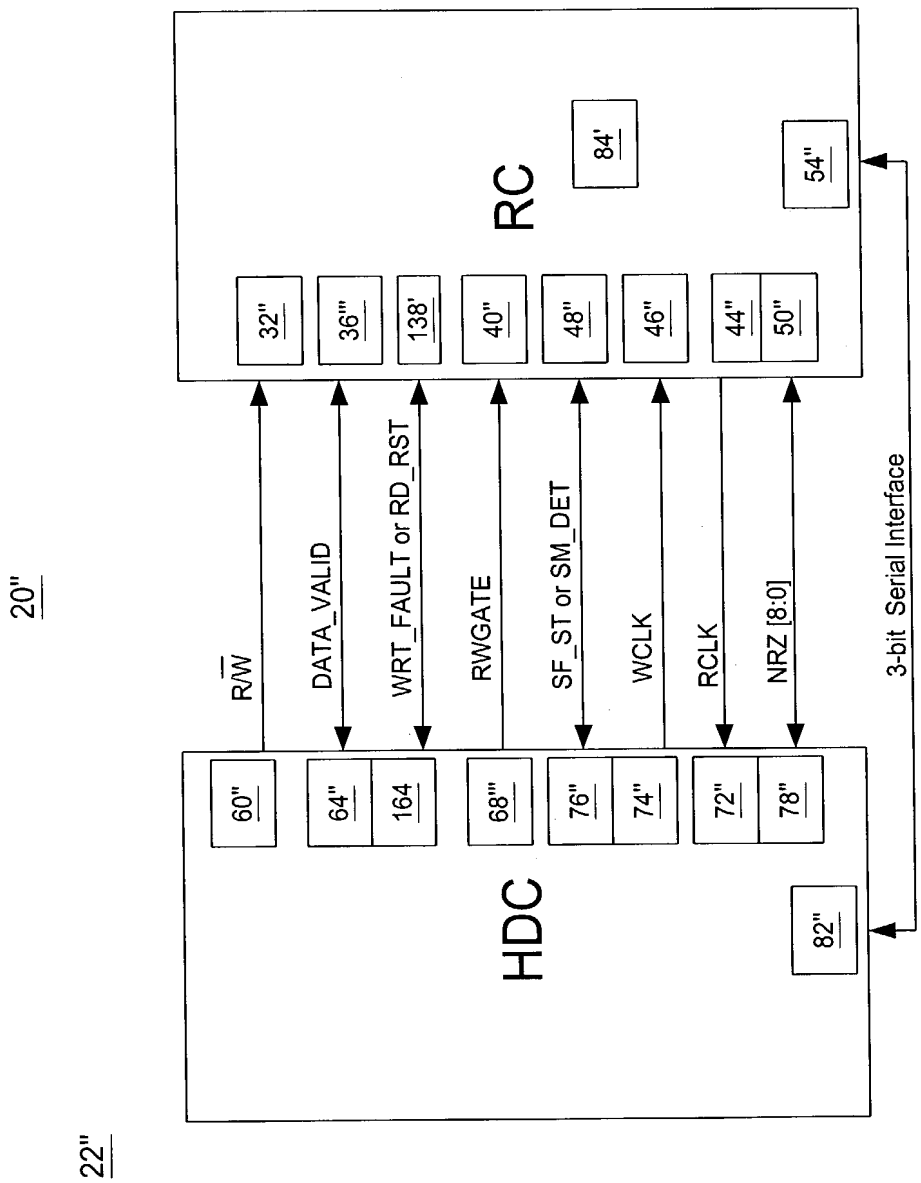

Fig. 25

09759151 .091902

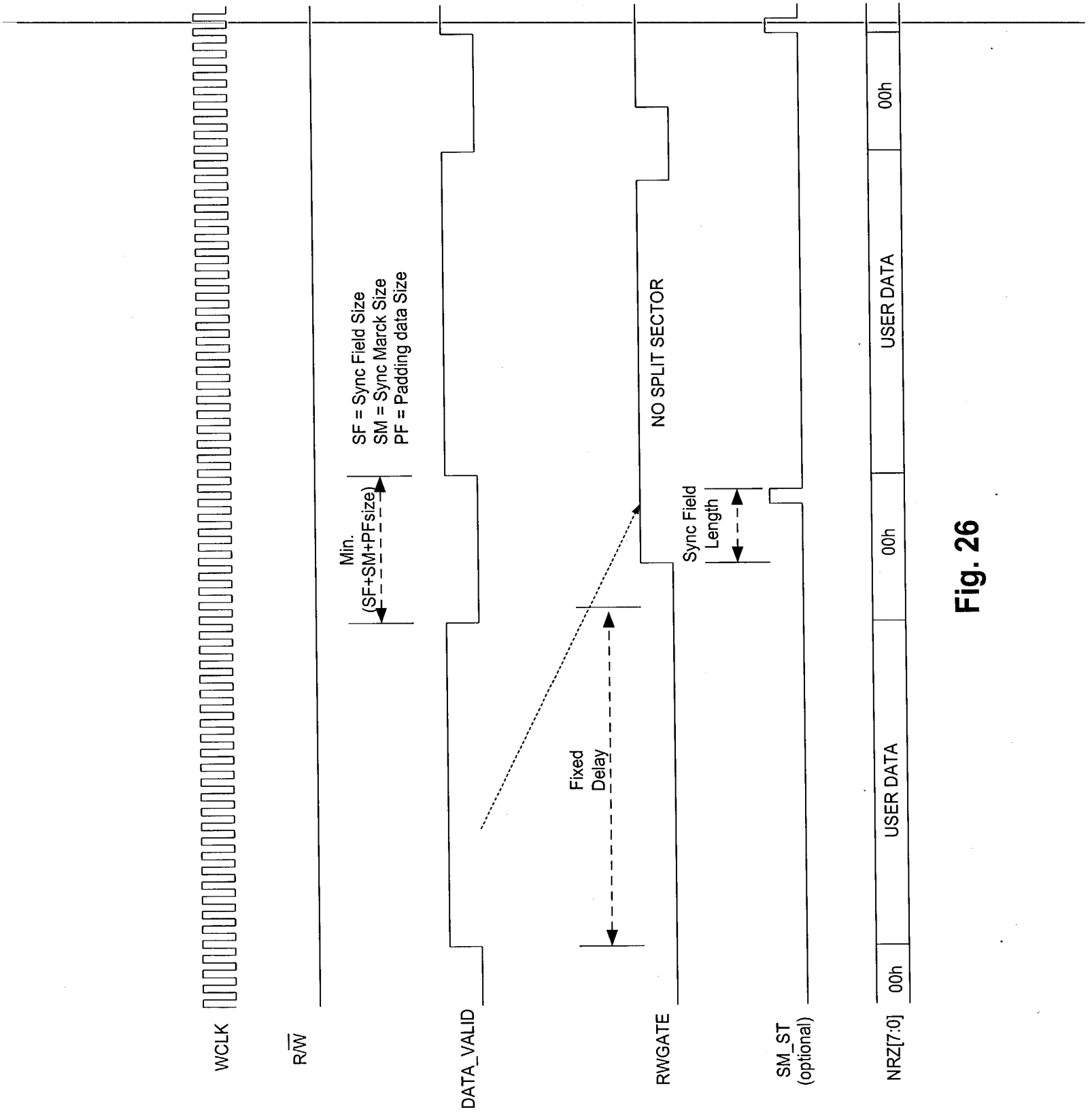

Fig. 26

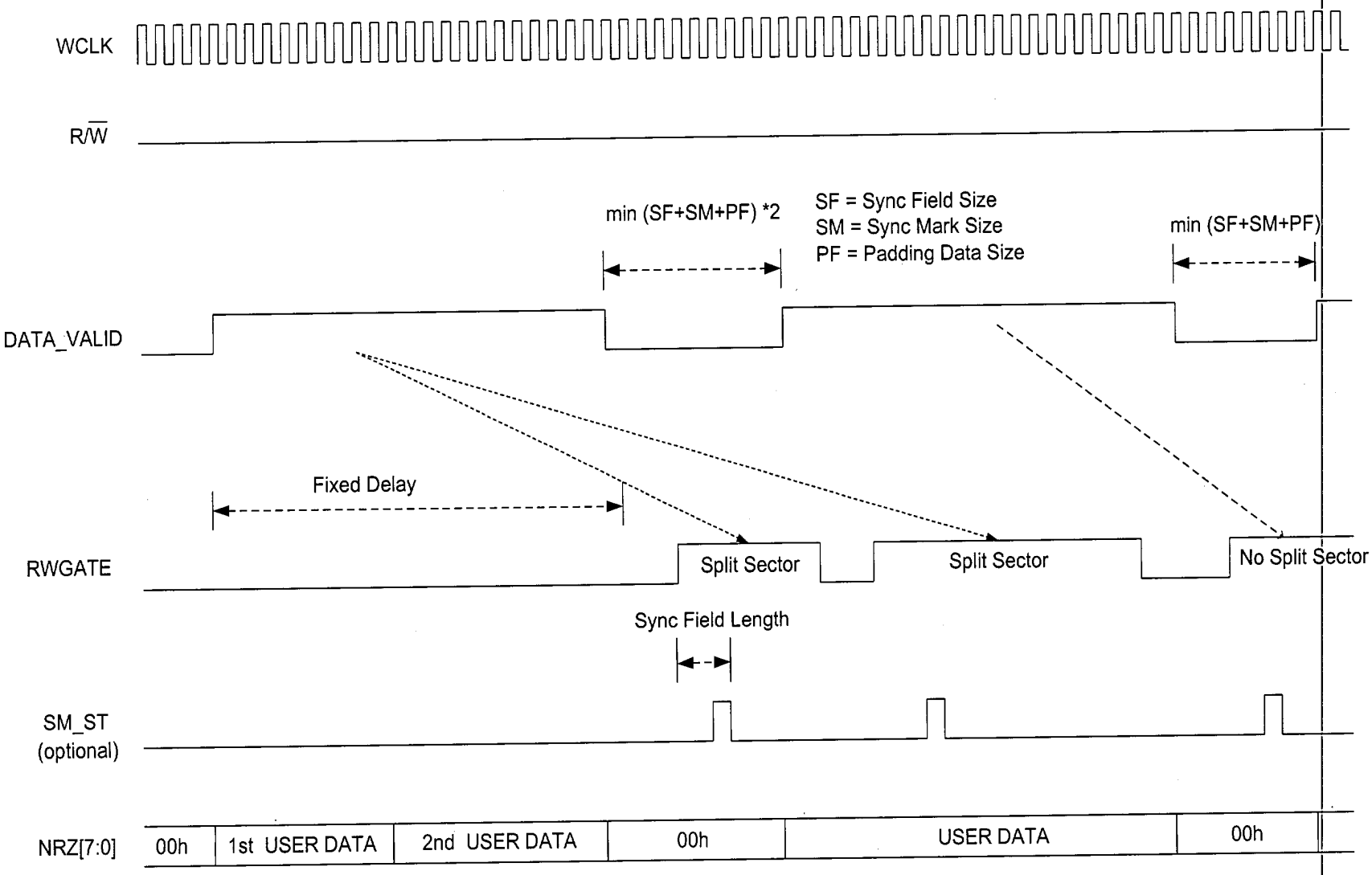
WCLK
R/W
min (SF+SM+PF) *2
SF = Sync Field Size
SM = Sync Mark Size
PF = Padding Data Size
min (SF+SM+PF)
DATA_VALID
Fixed Delay
RWGATE
Split Sector
Split Sector
No Split Sector
Sync Field Length
SM_ST
(optional)
NRZ[7:0]
00h
1st USER DATA
2nd USER DATA
00h
USER DATA
00h

Fig. 27

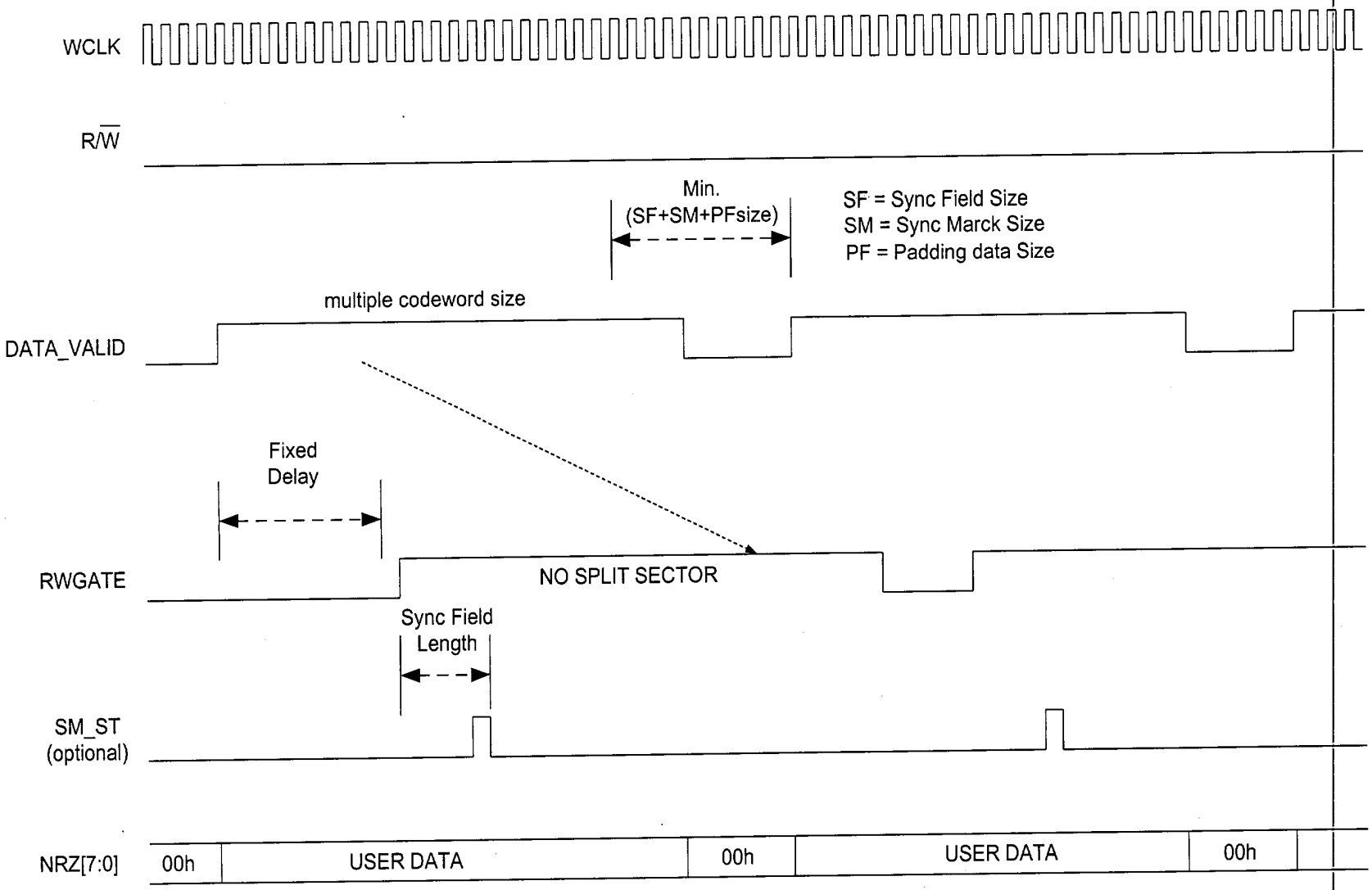
WCLK
R/W
Min.
(SF+SM+PFsize)
SF = Sync Field Size
SM = Sync Marck Size
PF = Padding data Size
multiple codeword size
DATA_VALID
Fixed
Delay
RWGATE
NO SPLIT SECTOR
Sync Field
Length
SM_ST
(optional)
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 28

09759151.091902

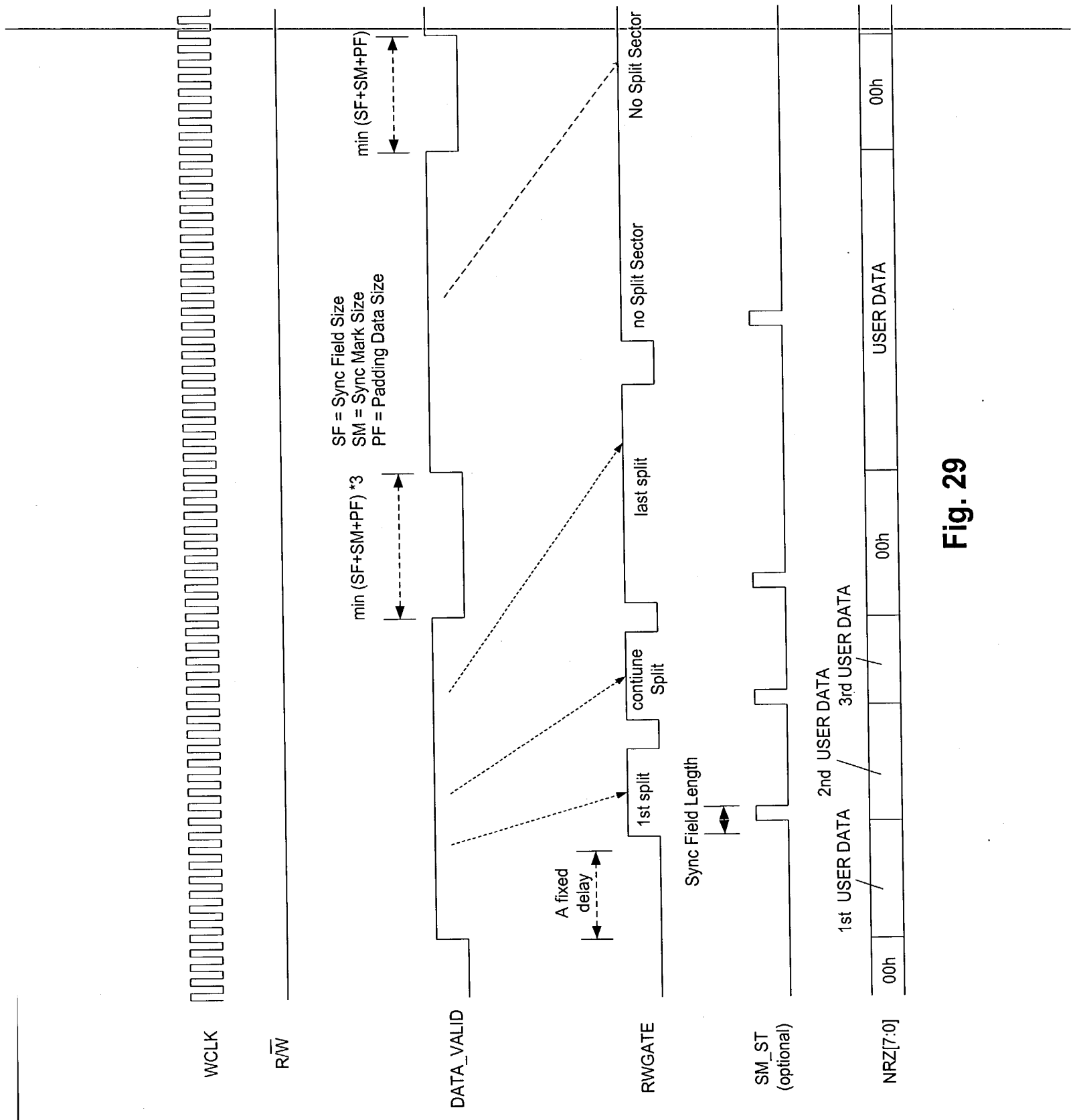

Fig. 29

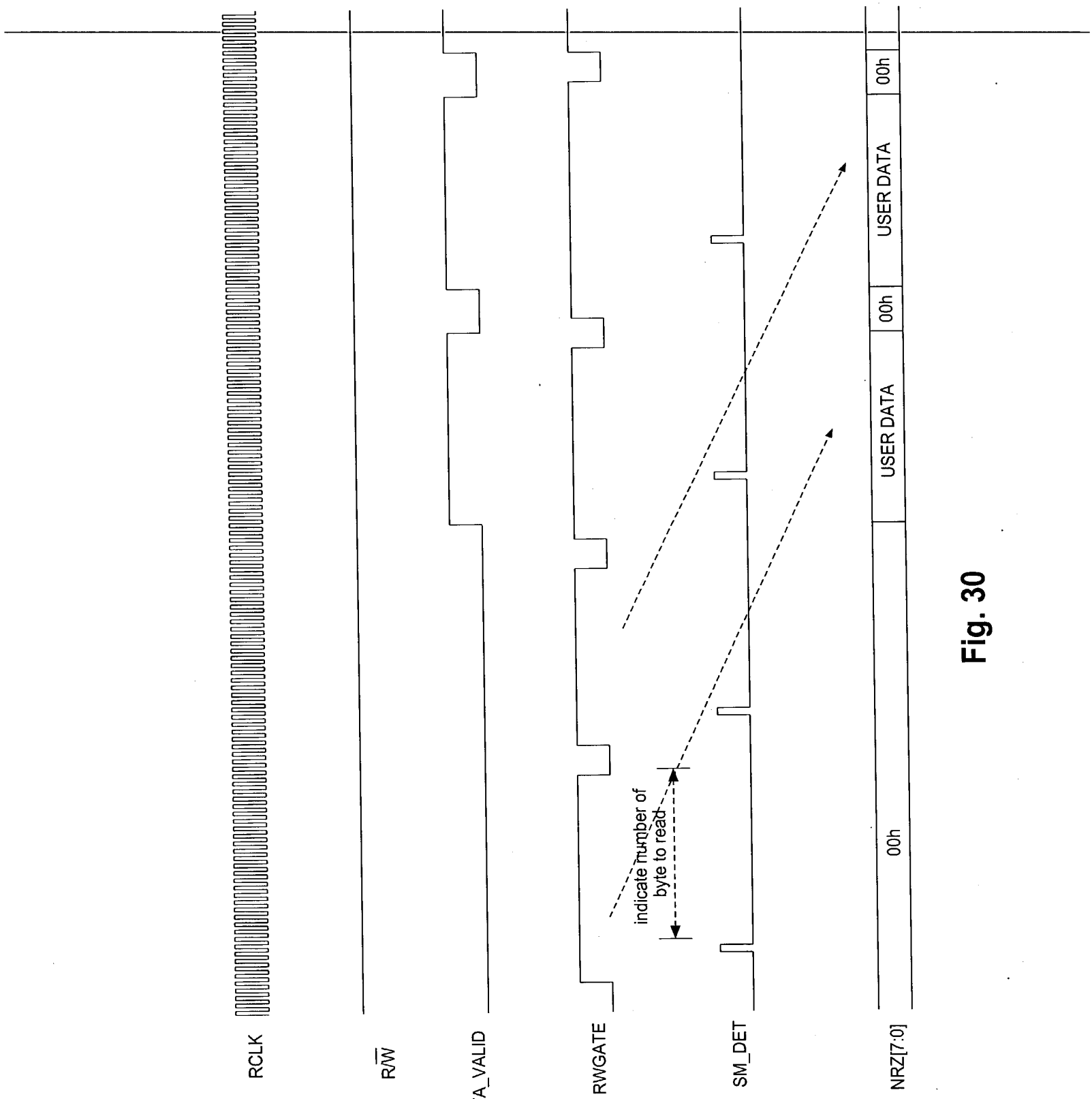
RCLK
R/W
DATA_VALID
RWGATE
SM_DET
NRZ[7:0]
indicate number of byte to read
00h
USER DATA
00h
USER DATA
00h

Fig. 30

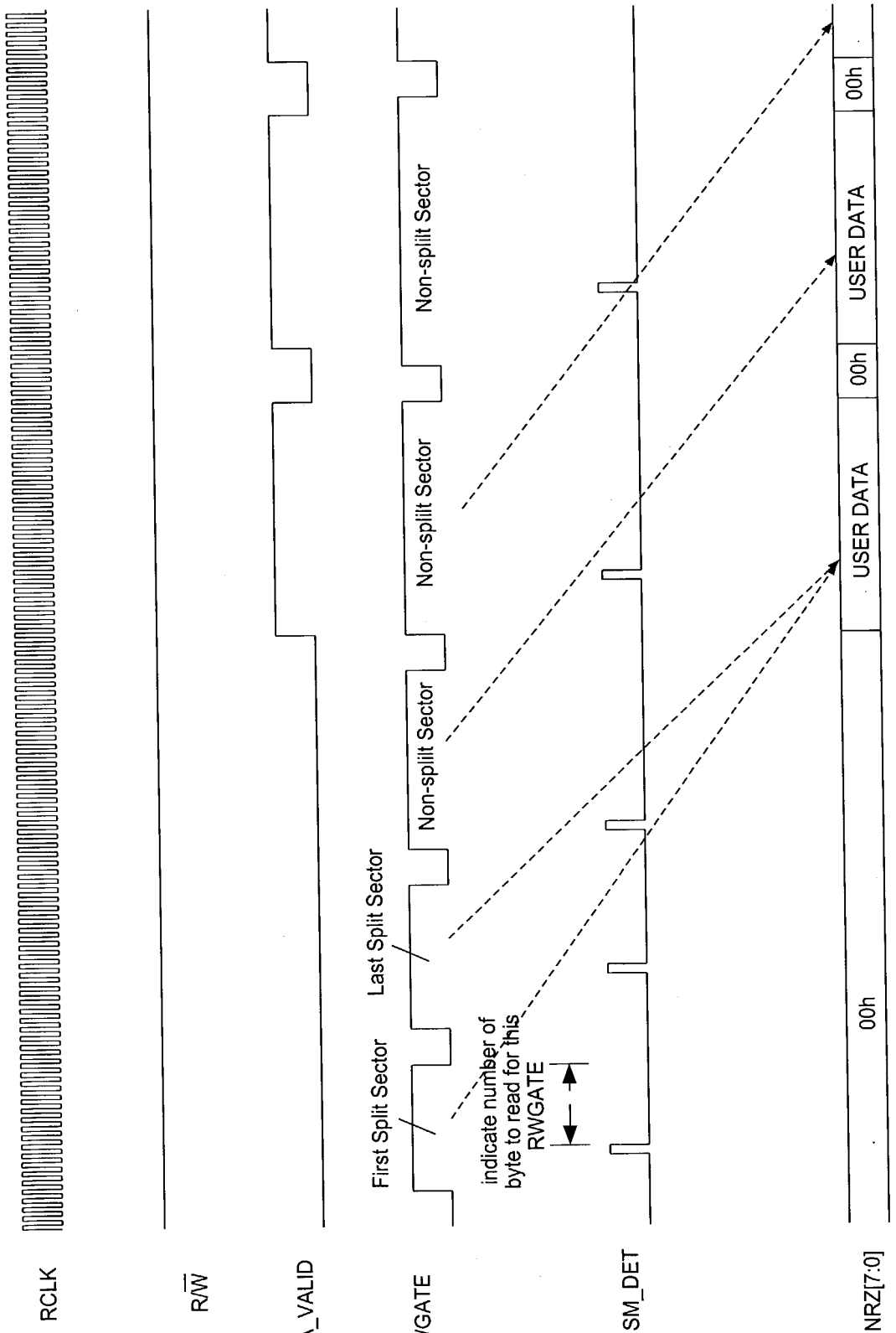
RCLK
R/W
DATA_VALID
RWGATE
SM_DET
NRZ[7:0]
First Split Sector
Last Split Sector
Non-split Sector
Non-split Sector
Non-split Sector
indicate number of byte to read for this RWGATE
00h
USER DATA
00h
USER DATA
00h

Fig. 31

09759151.091902

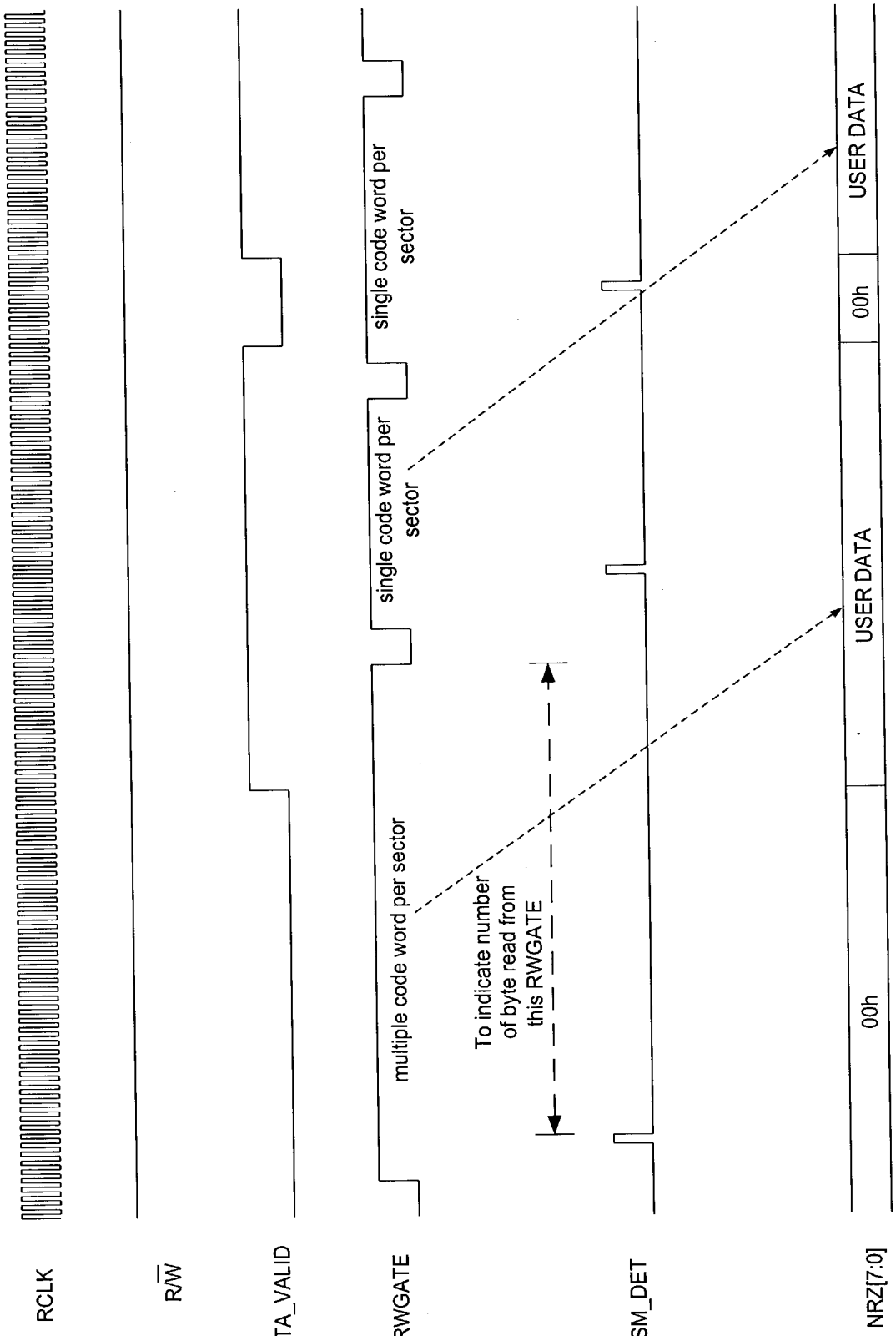

Fig. 32

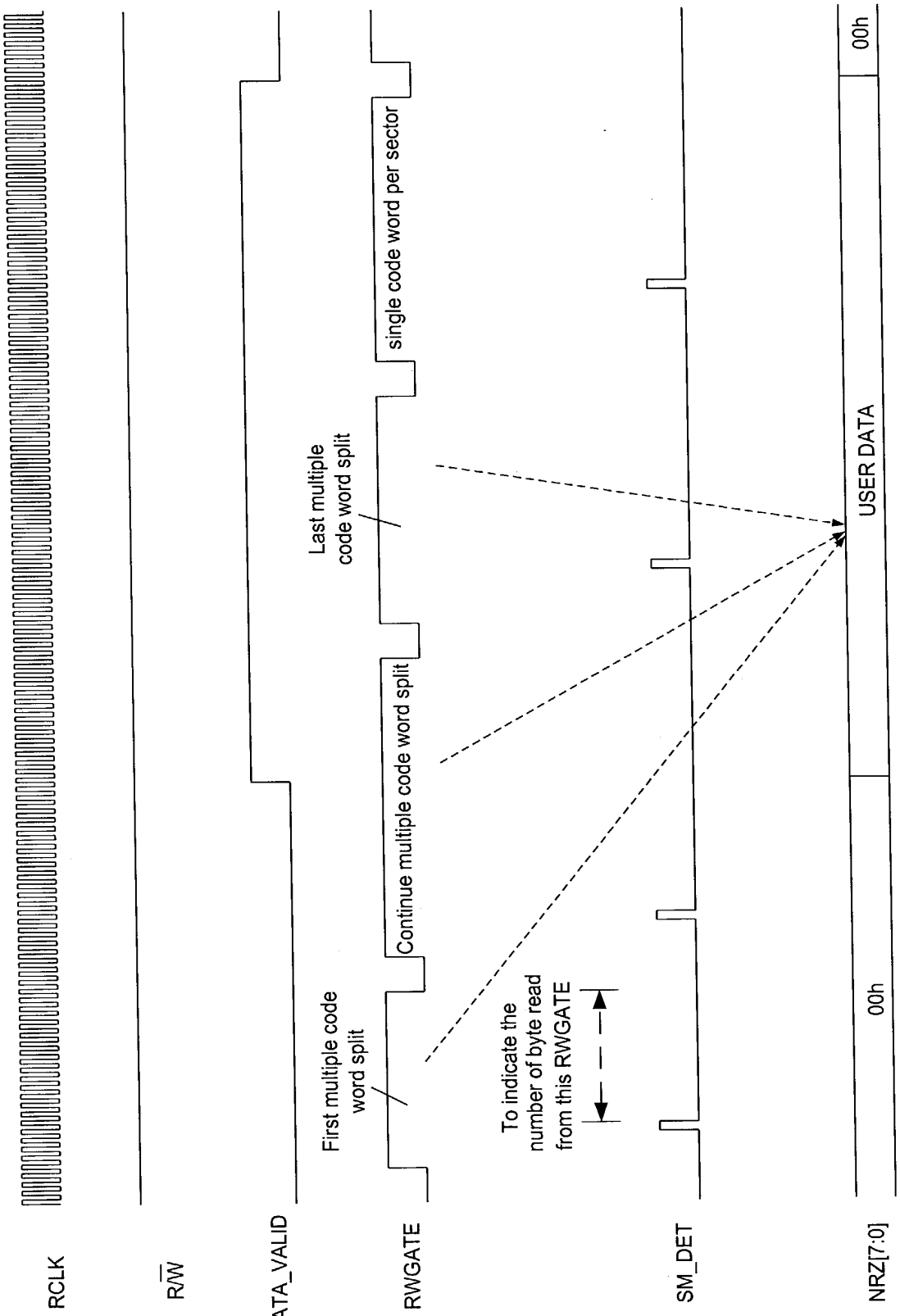
RCLK
R/W
DATA_VALID
RWGATE
SM_DET
NRZ[7:0]
First multiple code word split
Continue multiple code word split
Last multiple code word split
single code word per sector
To indicate the number of byte read from this RWGATE
00h
USER DATA
00h

Fig. 33

09759151.091902

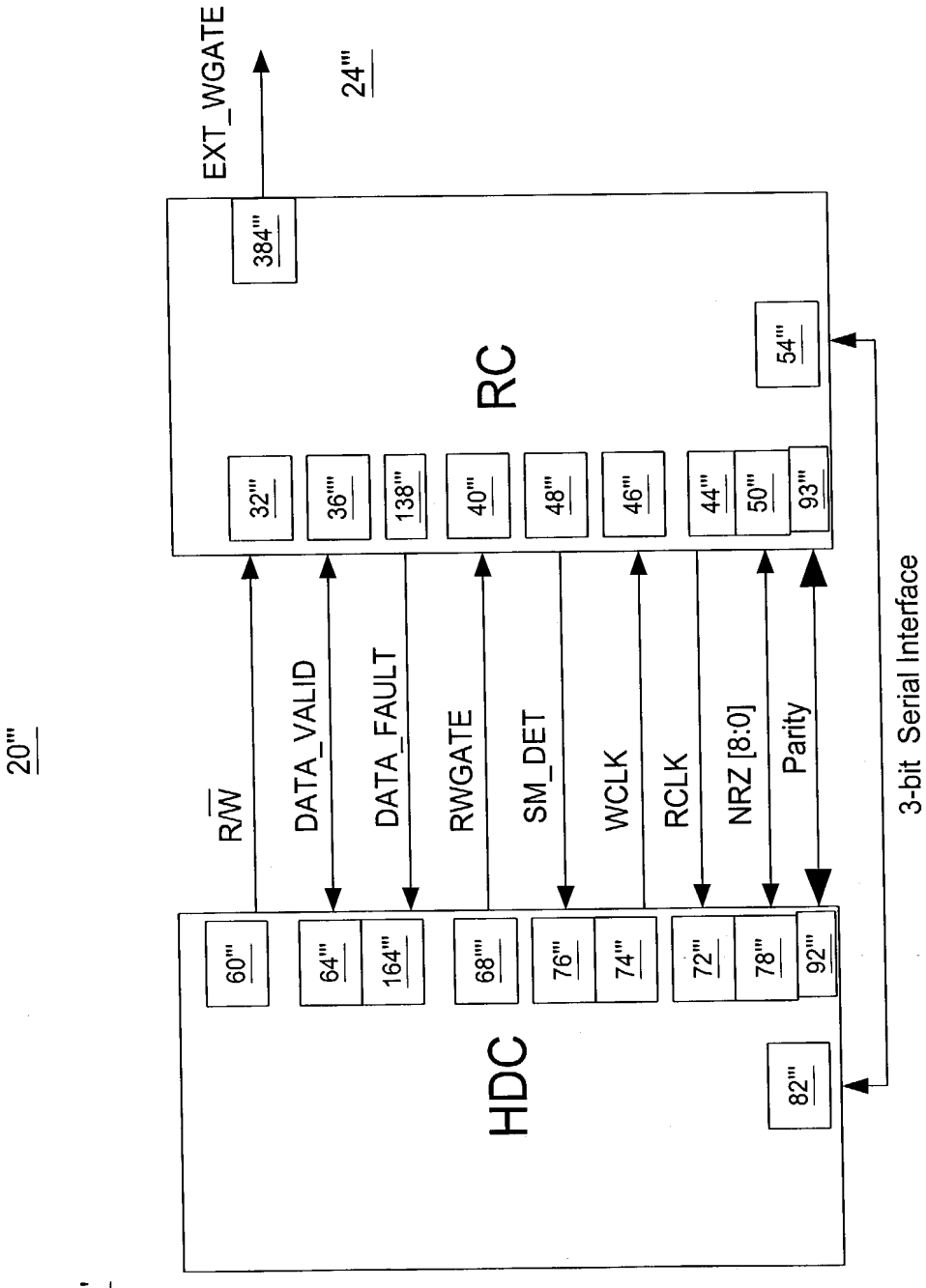

Fig. 34

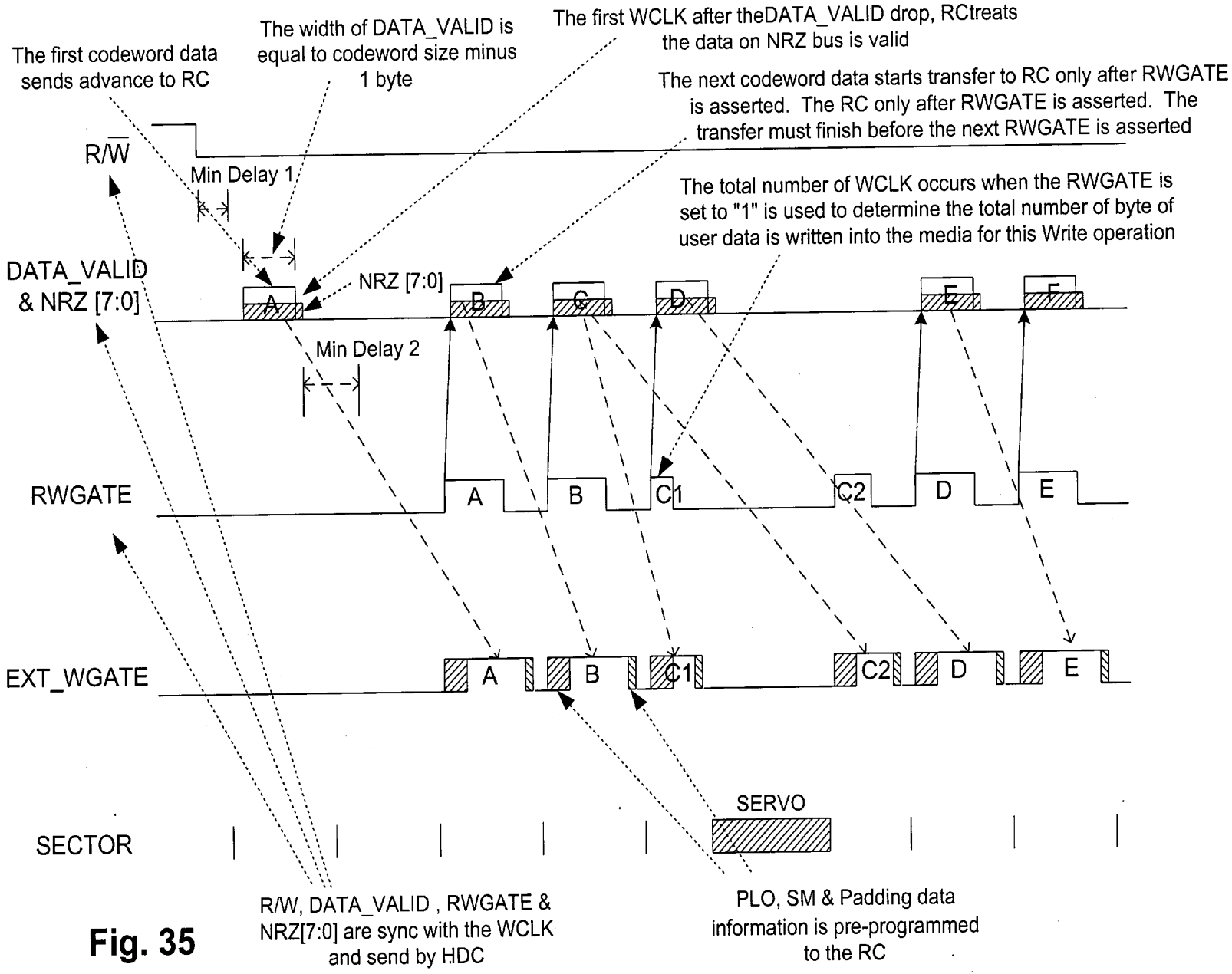
The first codeword data sends advance to RC
The width of DATA_VALID is equal to codeword size minus 1 byte
The first WCLK after theDATA_VALID drop, RCtreats the data on NRZ bus is valid
The next codeword data starts transfer to RC only after RWGATE is asserted. The RC only after RWGATE is asserted. The transfer must finish before the next RWGATE is asserted
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is written into the media for this Write operation
R/W
Min Delay 1
DATA_VALID & NRZ [7:0]
NRZ [7:0]
Min Delay 2
RWGATE
EXT_WGATE
SERVO
SECTOR
R/W, DATA_VALID , RWGATE & NRZ[7:0] are sync with the WCLK and send by HDC
PLO, SM & Padding data information is pre-programmed to the RC

Fig. 35

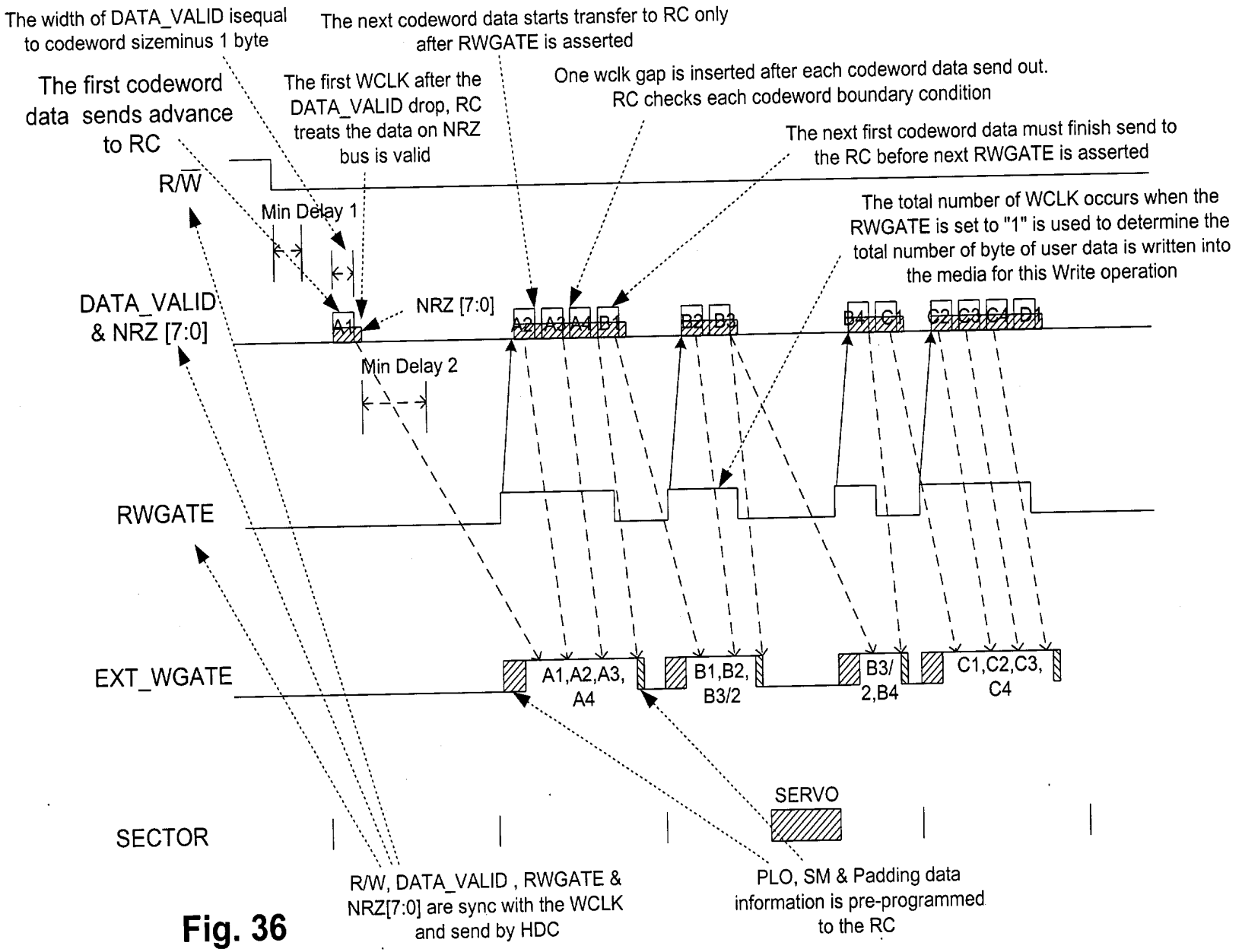
The width of DATA_VALID isequal to codeword sizeminus 1 byte
The next codeword data starts transfer to RC only after RWGATE is asserted
The first codeword data sends advance to RC
The first WCLK after the DATA_VALID drop, RC treats the data on NRZ bus is valid
One wclk gap is inserted after each codeword data send out. RC checks each codeword boundary condition
The next first codeword data must finish send to the RC before next RWGATE is asserted
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is written into the media for this Write operation
DATA_VALID & NRZ [7:0]
NRZ [7:0]
A1
A2 A3 A4 B1
B2 B3
B4 C1
C2 C3 C4 D1
Min Delay 2
RWGATE
EXT_WGATE
A1,A2,A3, A4
B1,B2, B3/2
B3/ 2,B4
C1,C2,C3, C4
SERVO
SECTOR
R/W, DATA_VALID , RWGATE & NRZ[7:0] are sync with the WCLK and send by HDC
PLO, SM & Padding data information is pre-programmed to the RC

Fig. 36

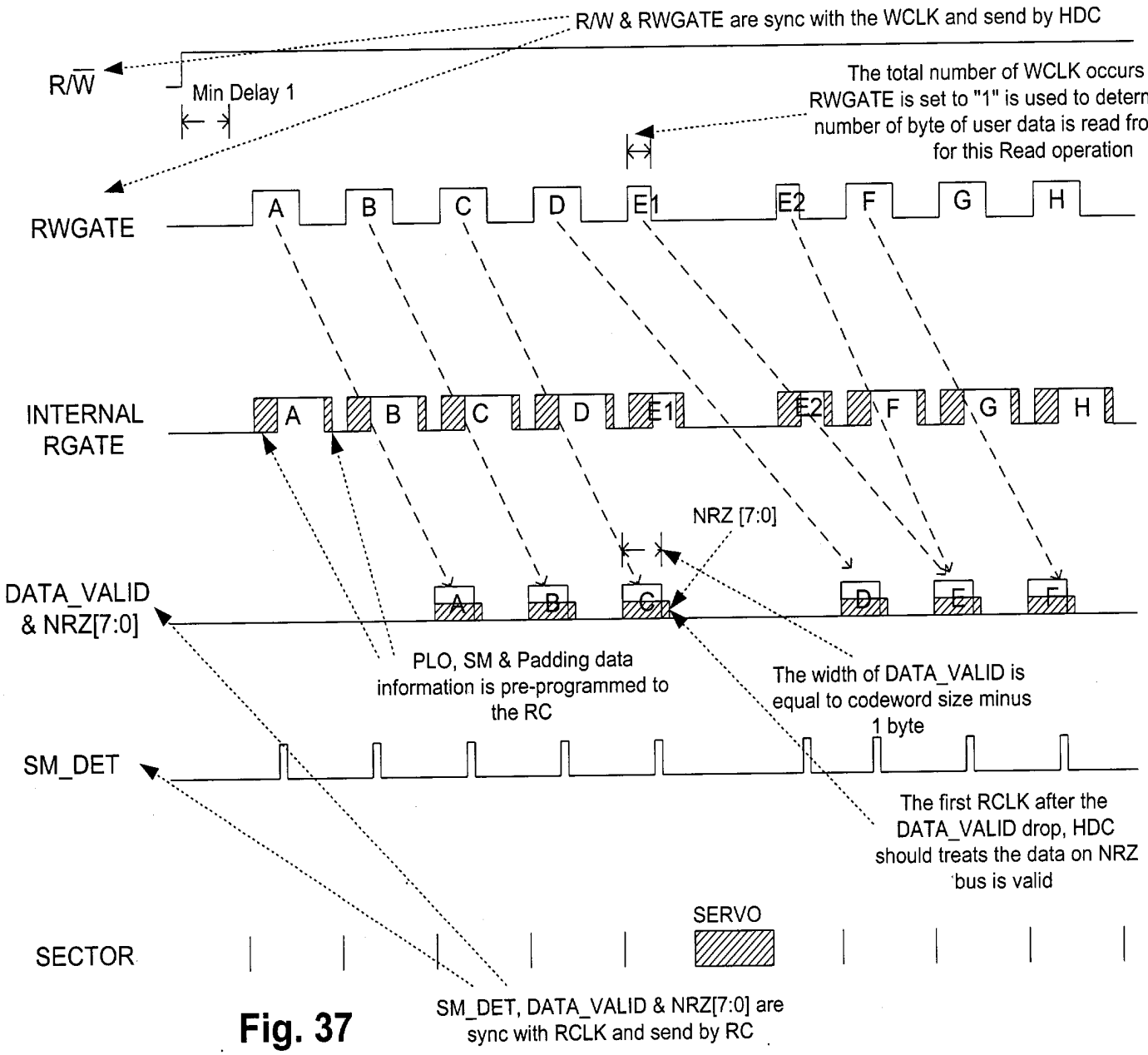
R/W & RWGATE are sync with the WCLK and send by HDC
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is read from the media for this Read operation
RWGATE
A
B
C
D
E1
E2
F
G
H
INTERNAL RGATE
NRZ [7:0]
DATA_VALID & NRZ[7:0]
PLO, SM & Padding data information is pre-programmed to the RC
The width of DATA_VALID is equal to codeword size minus 1 byte
SM_DET
The first RCLK after the DATA_VALID drop, HDC should treats the data on NRZ bus is valid
SERVO
SECTOR
SM_DET, DATA_VALID & NRZ[7:0] are sync with RCLK and send by RC

Fig. 37

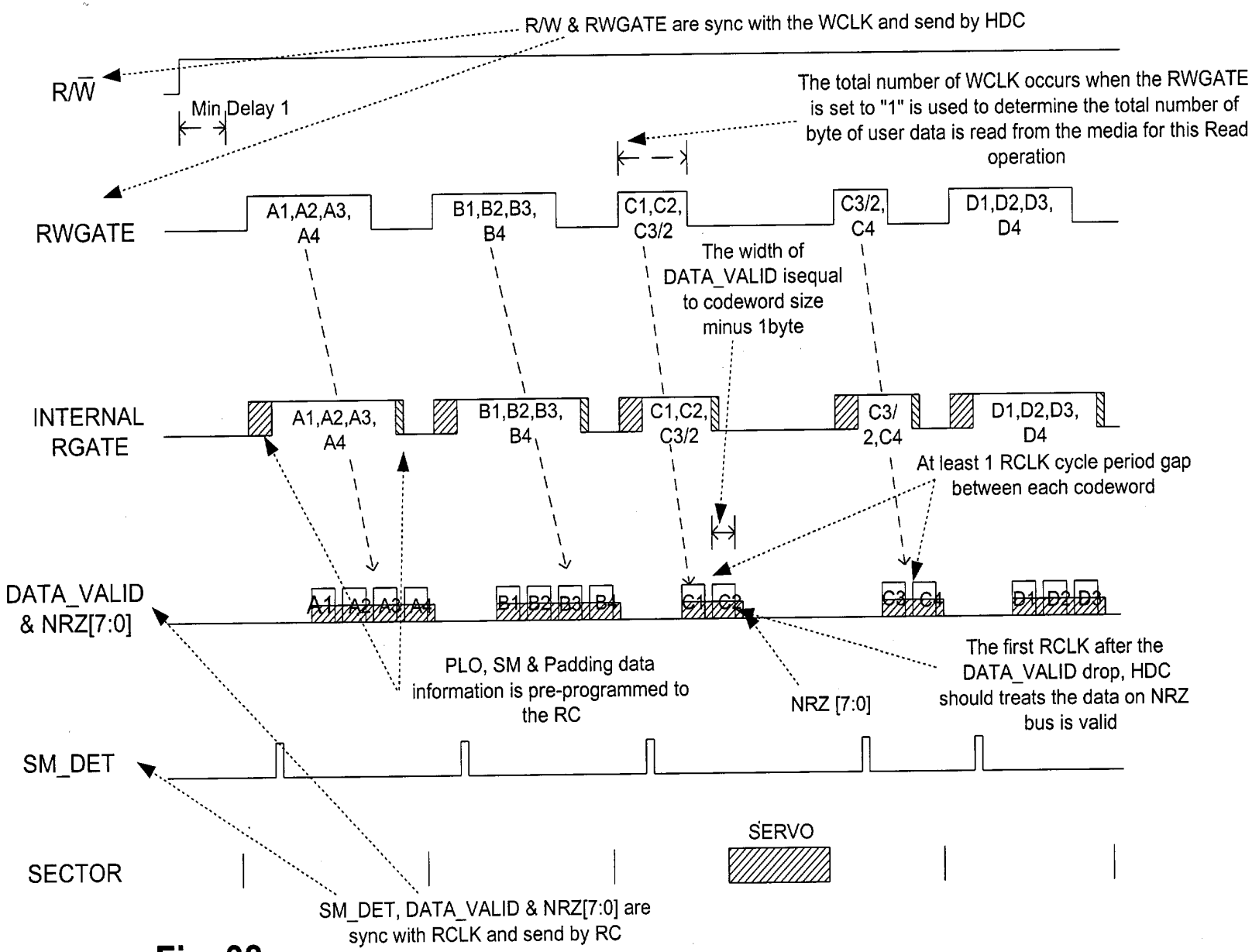
R/W & RWGATE are sync with the WCLK and send by HDC
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is read from the media for this Read operation
RWGATE
A1,A2,A3, A4
B1,B2,B3, B4
C1,C2, C3/2
C3/2, C4
D1,D2,D3, D4
The width of DATA_VALID isequal to codeword size minus 1byte
INTERNAL RGATE
A1,A2,A3, A4
B1,B2,B3, B4
C1,C2, C3/2
C3/ 2,C4
D1,D2,D3, D4
At least 1 RCLK cycle period gap between each codeword
DATA_VALID & NRZ[7:0]
PLO, SM & Padding data information is pre-programmed to the RC
NRZ [7:0]
The first RCLK after the DATA_VALID drop, HDC should treats the data on NRZ bus is valid
SM_DET
SERVO
SECTOR
SM_DET, DATA_VALID & NRZ[7:0] are sync with RCLK and send by RC

Fig. 38